# Chapter 17: Low-Power Design

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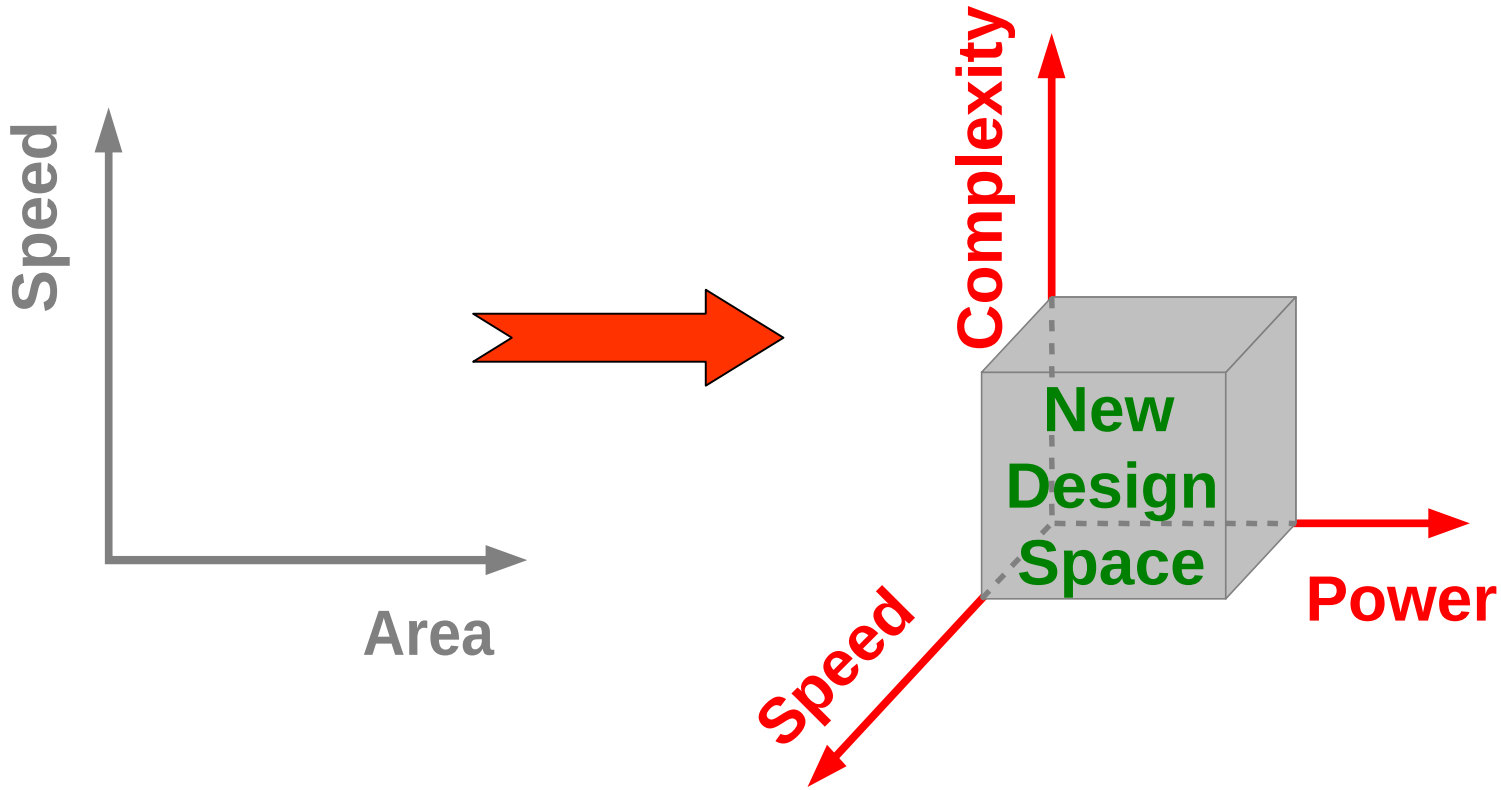
# IC Design Space



# VLSI Digital Signal Processing Systems

- Technology trends:
  - 200-300M chips by 2010 (0.07 micron CMOS)
- Challenges:
  - Low-power DSP algorithms and architectures
  - Low-power dedicated / programmable systems
  - Multimedia & wireless system-driven architectures
  - Convergence of Voice, Video and Data
  - LAN, MAN, WAN, PAN
  - Telephone Lines, Cables, Fiber, Wireless
  - Standards and Interoperability

# Power Consumption in DSP

- Low performance portable applications:
  - Cellular phones, personal digital assistants
  - Reasonable battery lifetime, low weight

- High performance portable systems:
  - Laptops, notebook computers
- Non-portable systems:
  - Workstations,  communication systems
  - DEC alpha: 1 GHz, 120 Watts
  - Packaging costs, system reliability

# Power Dissipation

**Two measures are important**

- **Peak power (Sets dimensions)**

$$P_{peak} = V_{DD} \times i_{DDmax}$$

- **Average power (Battery and cooling)**

$$P_{av} = \frac{V_{DD}}{T} \int_0^T i_{DD}(t)\, dt$$

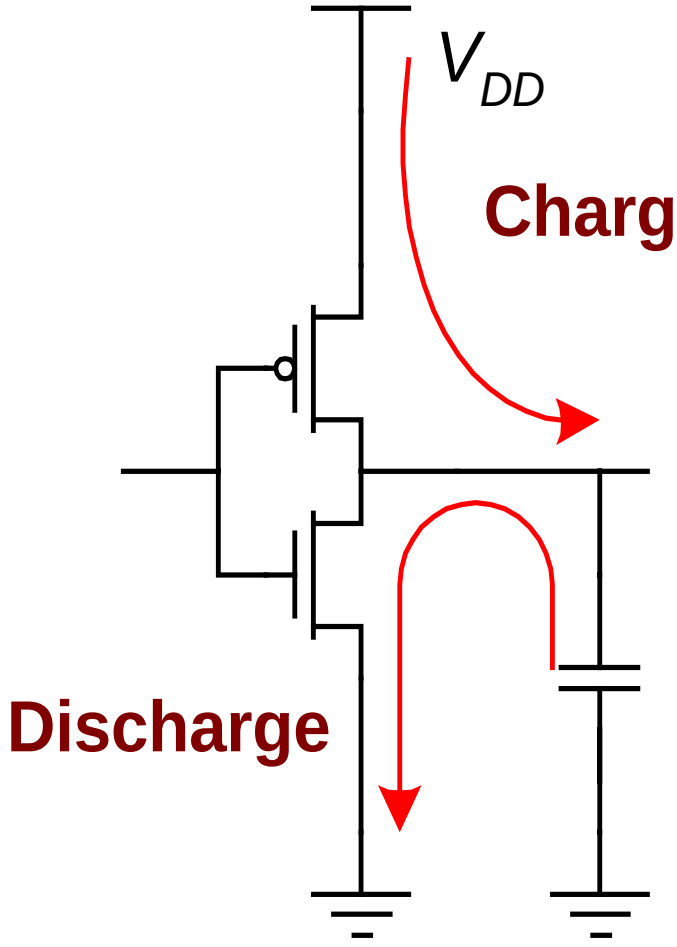
# CMOS Power Consumption

$$P_{tot} = P_{dyn} + P_{sc} + P_{leakage} =$$

$$= \alpha f C_L V_{DD}^2 \quad + \quad V_{DD} I_{sc} + \quad I_{leakage} V_{DD}$$

$\alpha$ = probability for switching

# Dynamic Power Consumption




**Energy charged in a capacitor**

$$E_C = CV^2/2 = C_L V_{DD}^2/2$$

**Energy $E_c$ is also discharged, i.e.**

$$E_{tot} = C_L V_{DD}^2$$

**Power consumption**

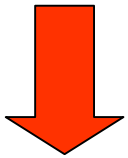
$$P = C_L V_{DD}^2 f$$

Off-Chip Connections have High Capacitive Load

Reduced off Chip Data Transfers by

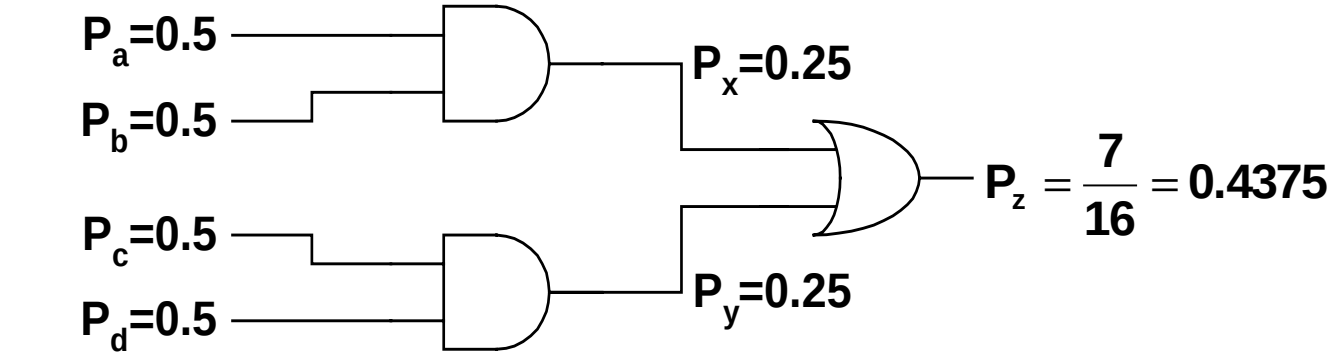
System Integration

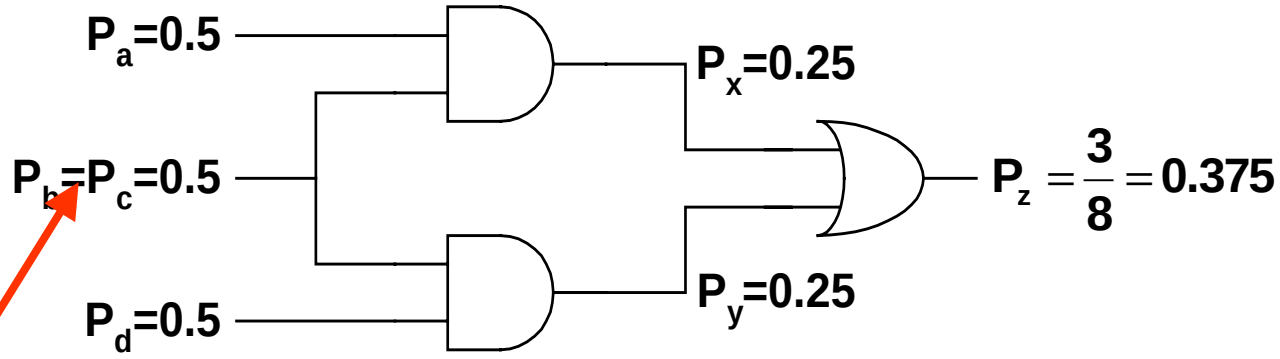
Ideally a Single Chip Solution



Reduced Power Consumption

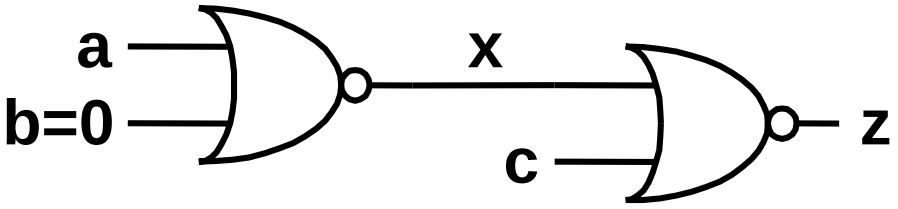
# Switching Activity ($\alpha$): Example

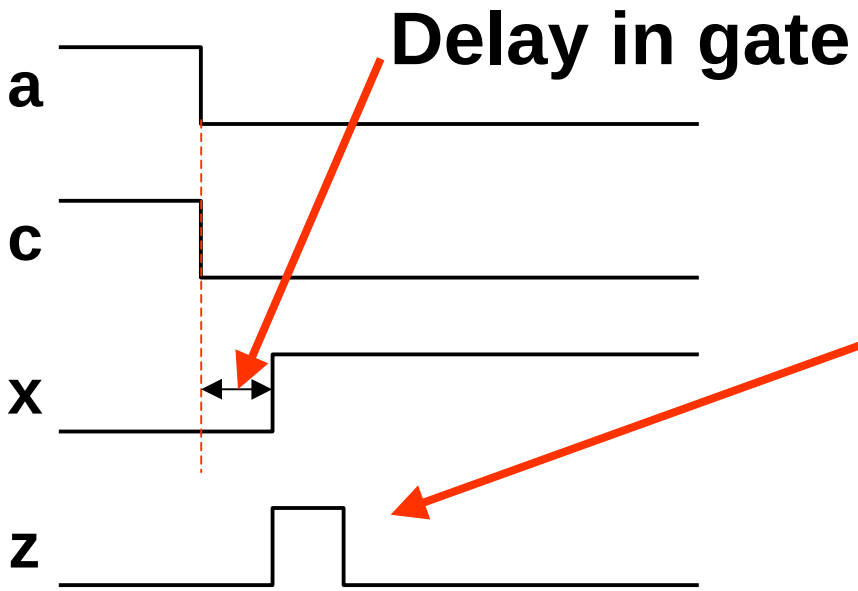



**Due to correlation**

# Increased Switching Activity due to Glitching

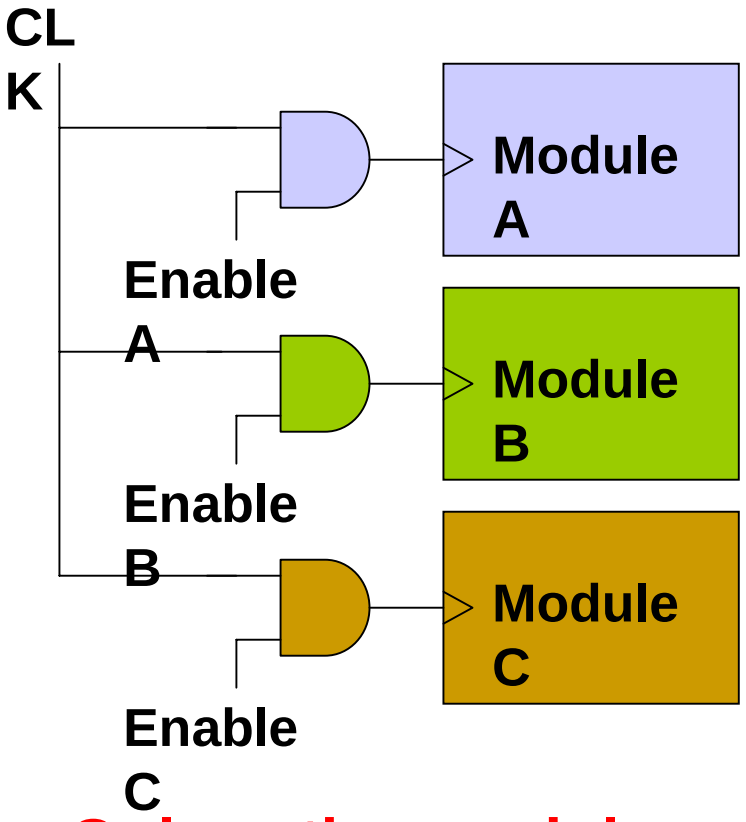



**Extra transition due to race**

**Dissipates energy**

# Clock Gating and Power Down



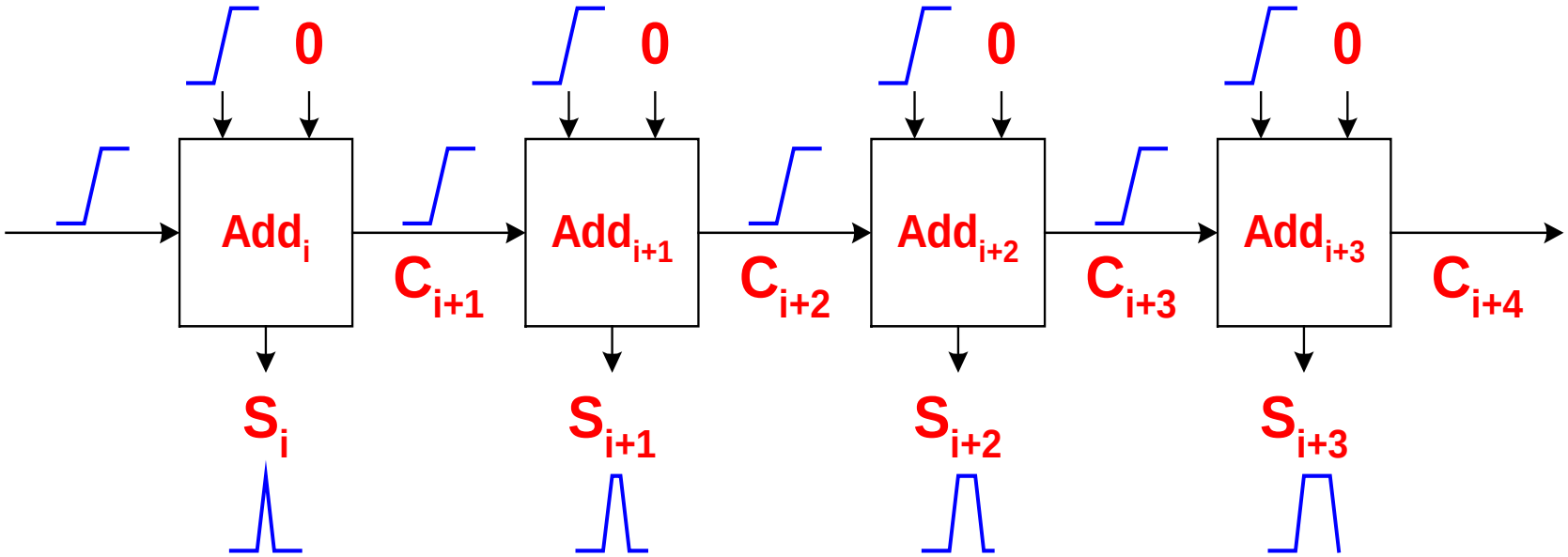

**Control circuitry is needed for clock gating and power down**

**and**

**Needs wake-up**

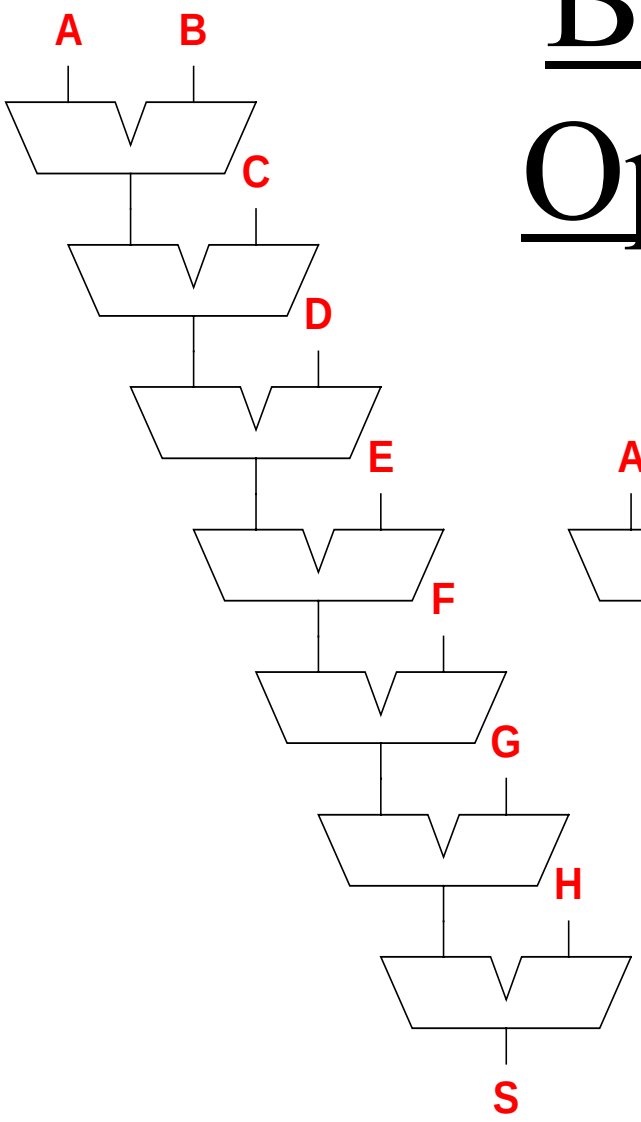
**Only active modules should be clocked!**

# Carry Ripple

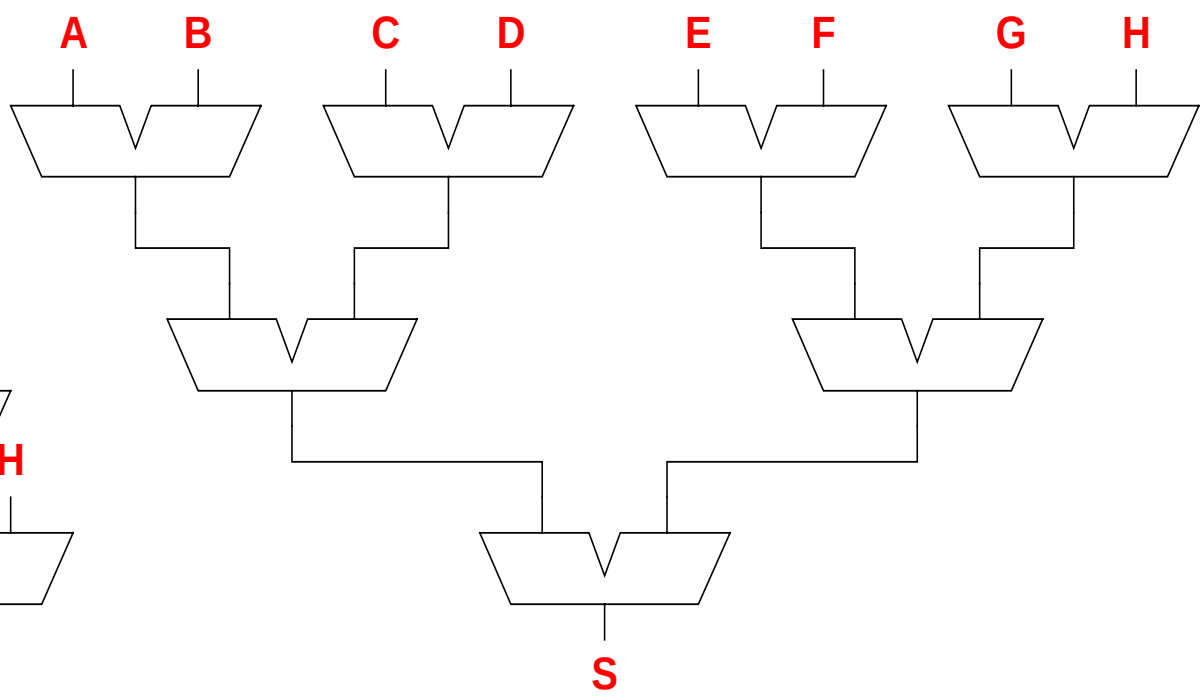



**Transitions due to carry propagation**

# Balancing Operations




**Example: Addition**



# Delay as function of Supply

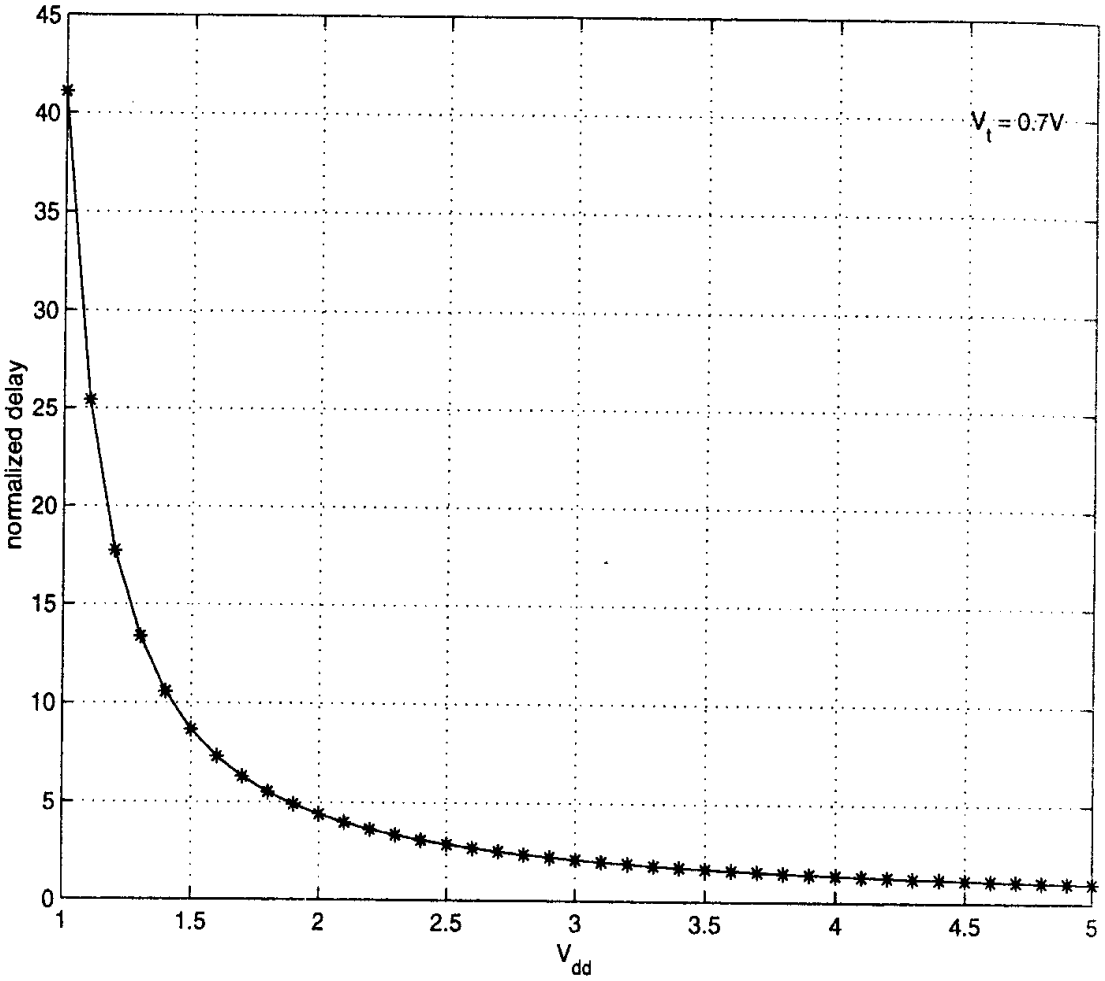



*Fig. 17.3* Circuit delay as a function of supply voltage.

# Delay as function of Threshold

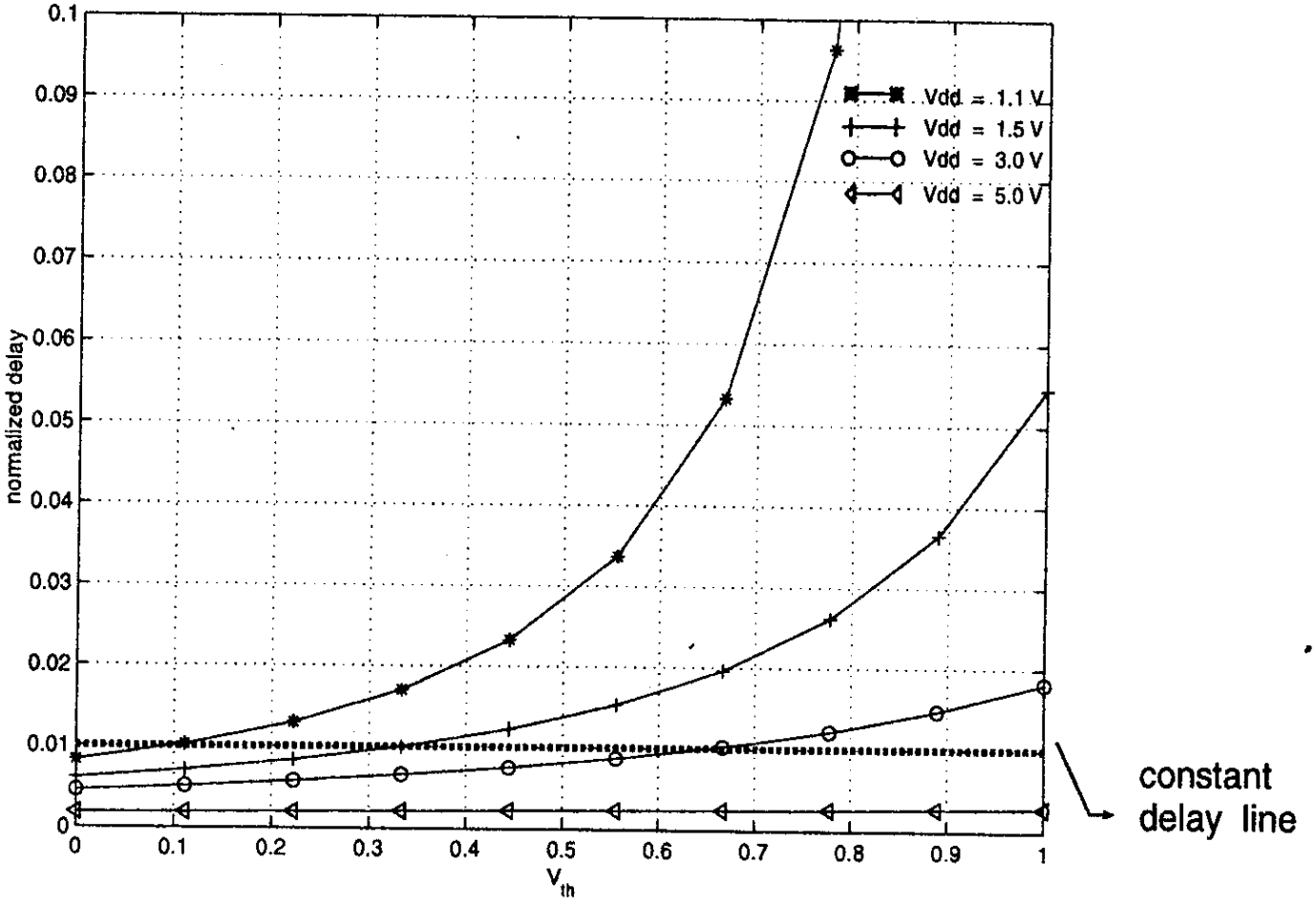
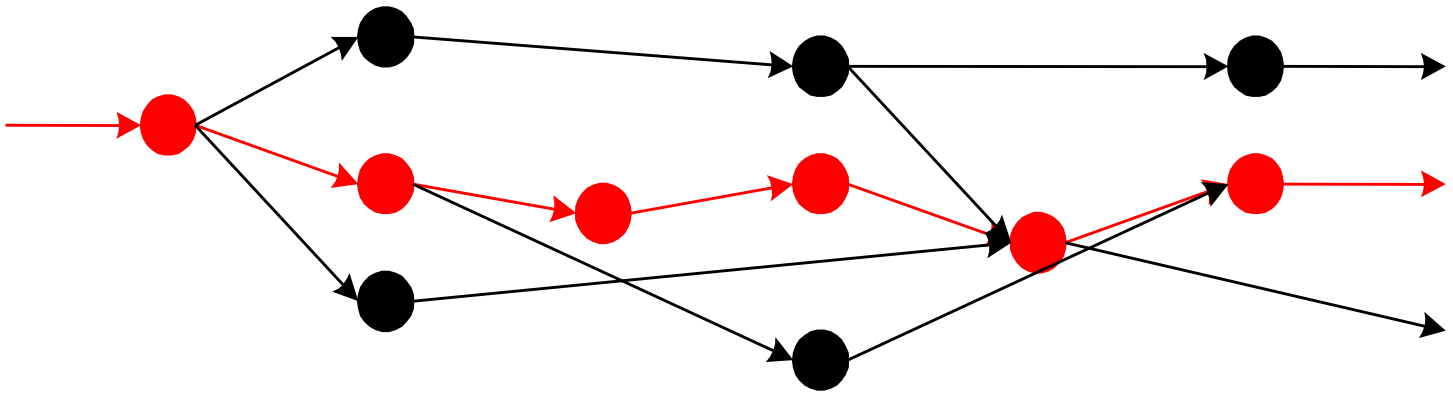



*Fig. 17.4* Circuit delay as a function of supply voltage for varying threshold voltages.

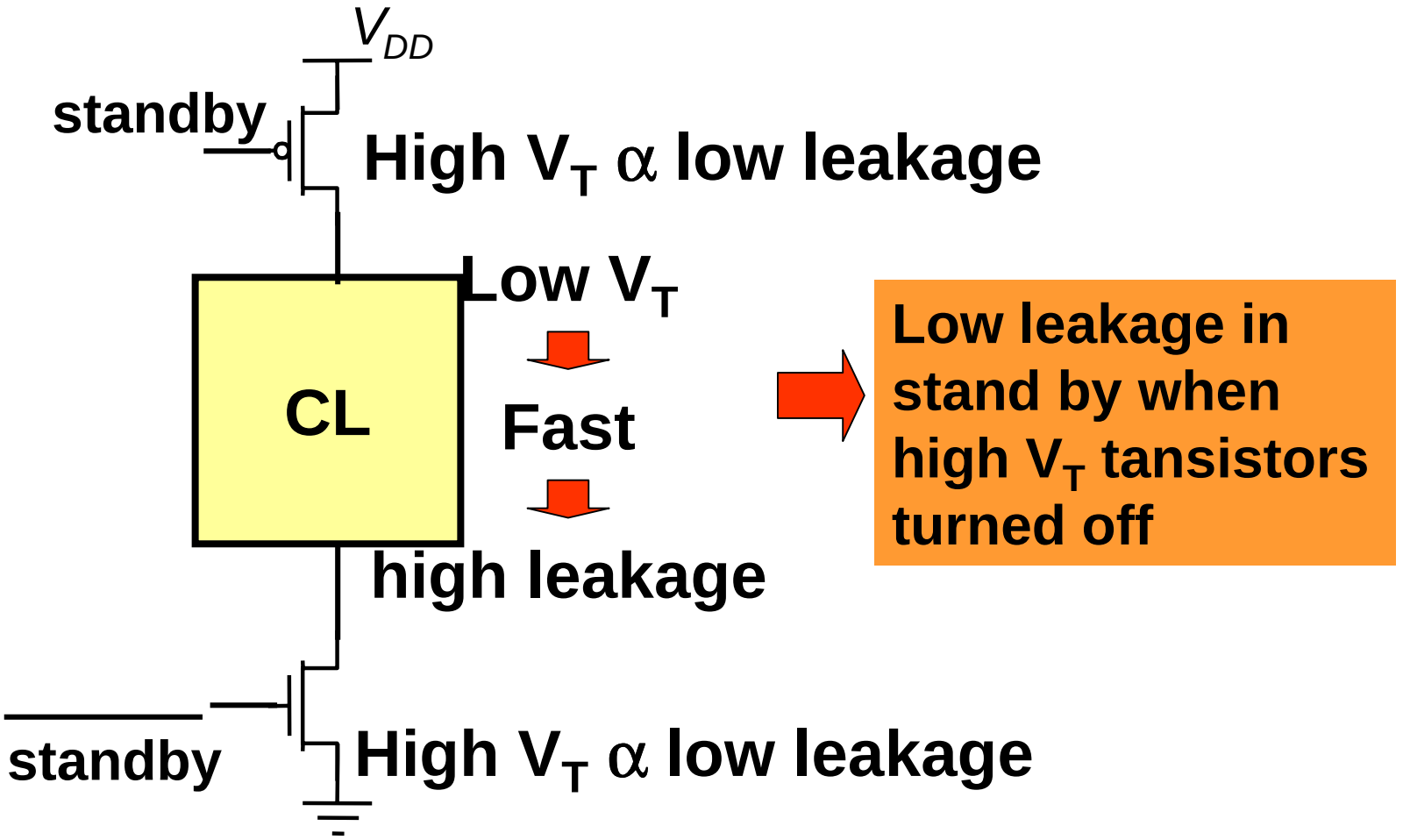
# Dual $V_T$ Technology

**Reduced $V_{DD}$ $\alpha$ Increased delay**
**Low $V_T$ $\alpha$ Faster but Increased Leakage**

## Low $V_T$ in critical path

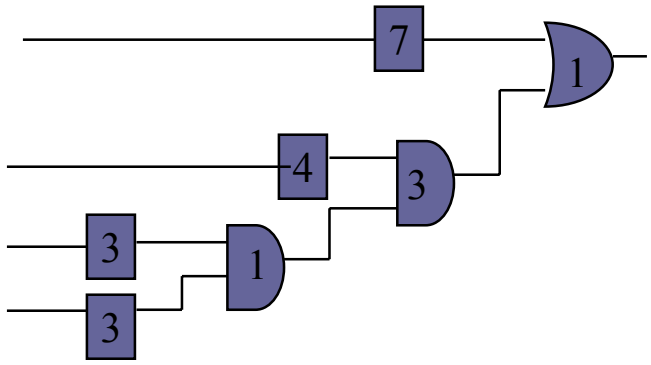


# High $V_T$ stand-by

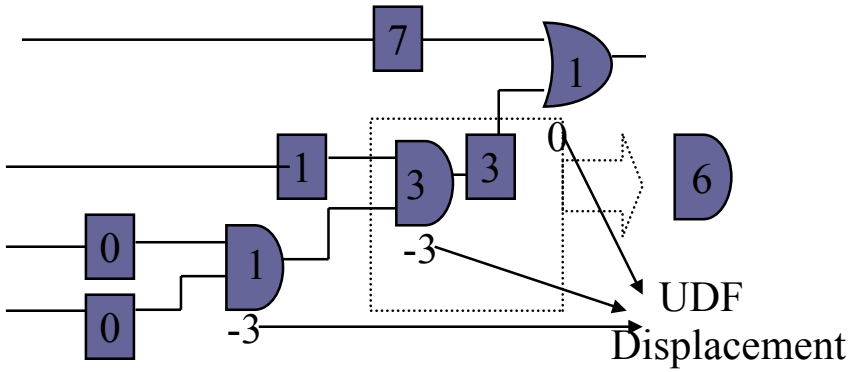


# Low Power Gate Resizing

- Systematic capture and elimination of slack using fictitious entities called *Unit Delay Fictitious Buffers.*
- Replace unnecessary fast gates by slower lower power gates from an underlying gate library.
- Use a simple relation between a gate's speed and power and the UDF's in its fanout nets. Model the problem as an *efficiently solvable ILP* similar to retiming.
- In *Proceedings of ARVLSI'99* Georgia Tech.




Critical Path = 8, UDF's in Boxes




Critical Path = 8, UDF's in Boxes

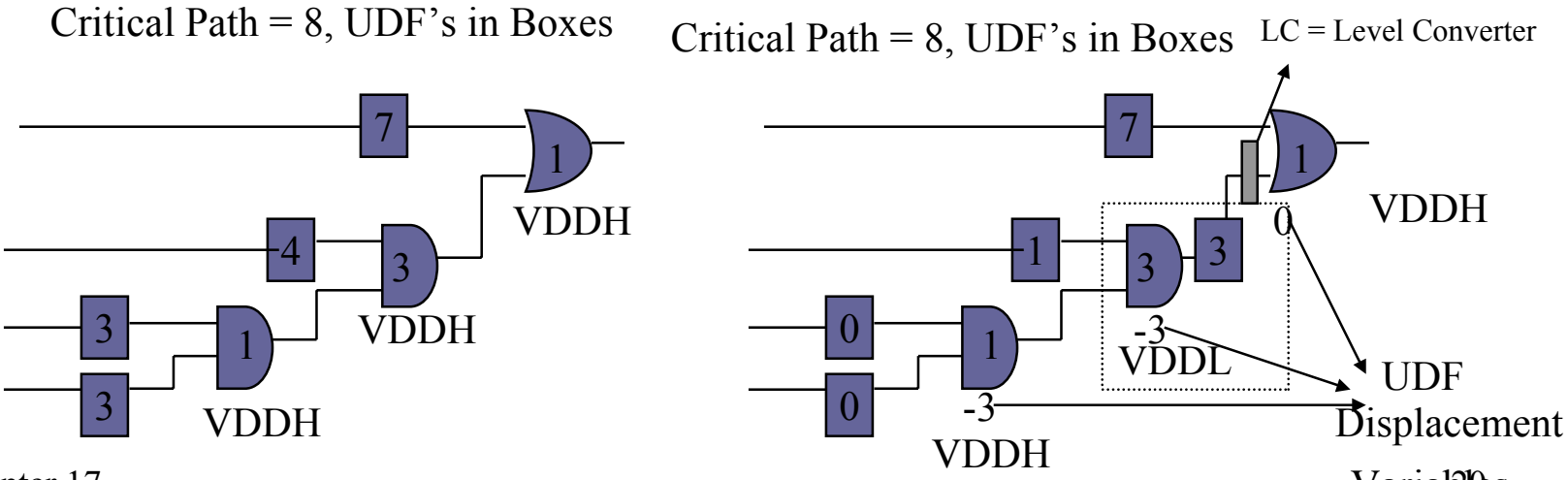
# Dual Supply Voltages for Low Power

- Components on the Critical Path exhibit no slack but components off the critical path exhibit excessive slack.
- A high supply voltage VDDH for critical path components and a low supply voltage VDDL for non critical path components.
- Throughput is maintained and power consumption is lowered.

V. Sundararajan and K.K. Parhi, "Synthesis of Low Power CMOS VLSI Circuits using Dual Supply Voltages", Prof. of ACM\/IEEE Design Automation Conference, pp. 72-75, New Orleans, June 1999

# Dual Supply Voltages for Low Power

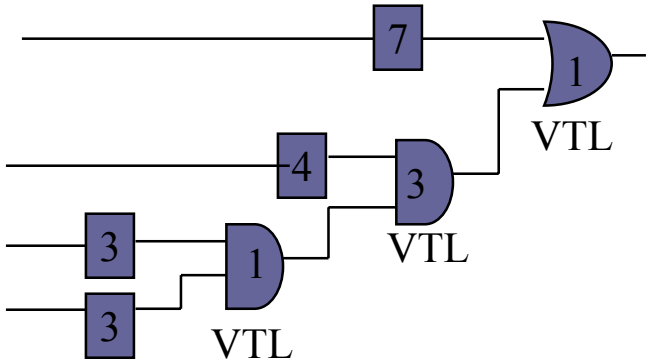
- Systematic capture and elimination of slack using fictitious entities called *Unit Delay Fictitious Buffers.*
- Switch unnecessarily fast gates to to lower supply voltage VDDL thereby saving power, critical path gates have a high supply voltage of VDDH.
- Use a simple relation between a gate's speed/power and supply voltage with the UDF's in its fanout nets. Model the problem as an *approximately solvable ILP*.

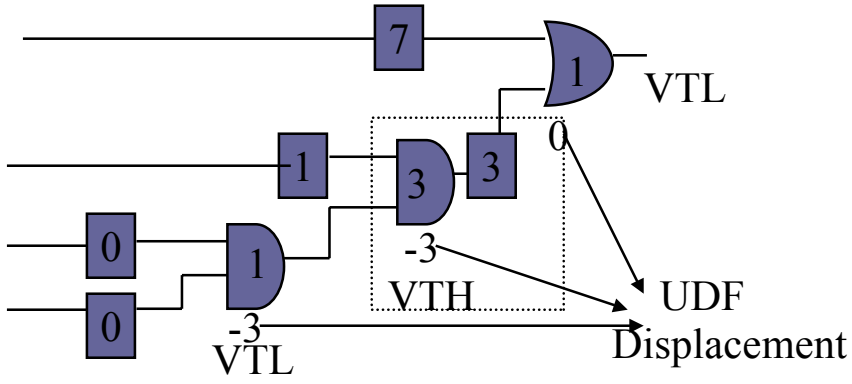


# Dual Threshold CMOS VLSI for Low Power

- Systematic capture and elimination of slack using fictitious entities called *Unit Delay Fictitious Buffers.*
- Gates on the critical path have a low threshold voltage VTL and unnecessarily fast gates are switched to a high threshold voltage VTH.
- Use a simple relation between a gate's speed /power and threshold voltage with the UDF's in its fanout nets. Model the problem as an *efficiently approximable 0-1 ILP.*

Critical Path = 8, UDF's in Boxes




Critical Path = 8, UDF's in Boxes

# Experimental Results

- Table :ISCAS'85 Benchmark Ckts Resizing (20 Sizes) Dual VDD Dual

| | | | | (5v, 2.4v) | | Vt |
|---|---|---|---|---|---|---|
| Ckt | #Gates | Power Savings | CPU(s) | Power Savings | CPU(s) | Power Savings |
| C1908 | 880 | 15.27% | 87.5 | 49.5% | 739.05 | 84.92% |
| c2670 | 1211 | 28.91% | 164.38 | 57.6% | 1229.37 | 90.25% |
| c3540 | 1705 | 37.11% | 312.51 | 57.7% | 1743.75 | 83.36% |
| c5315 | 2351 | 41.91% | 660.56 | 62.4% | 4243.63 | 91.56% |
| c6288 | 2416 | 5.57% | 69.58 | 62.7% | 7736.05 | 61.75% |
| c7552 | 3624 | 54.05% | 1256.76 | 59.6% | 9475.1 | 90.90% |

V. Sundararajan and K.K. Parhi, "Low Power Synthesis of Dual Threshold Voltage CMOS VLSI Circuits" Proc. of 1999 IEEE Int. Symp. on Low-Power Electronics and Design, pp. 139-144, San Diego, Aug. 1999

# HEAT: Hierarchical Energy Analysis Tool

- Salient features:
  - Based on stochastic techniques
  - Transistor-level analysis
  - Effectively models glitching activity
  - Reasonably fast due to its hierarchical nature

# Theoretical Background

- Signal probability:
  - S=$T_{clk}$ / $T_{gd}$ ,where
    $T_{clk}$ :clock period
    $T_{gd}$ : smallest gate delay
- Transition probability:
- Conditional probability:

$$p_{x_i}^1 = \lim_{N\to\infty} \frac{\sum_{j=1}^{NS} x_i(j)}{NS}$$

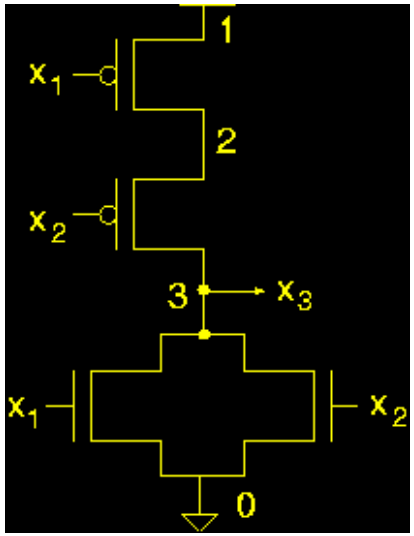
$$p_{x_i}^0 = 1 - p_{x_i}^1$$

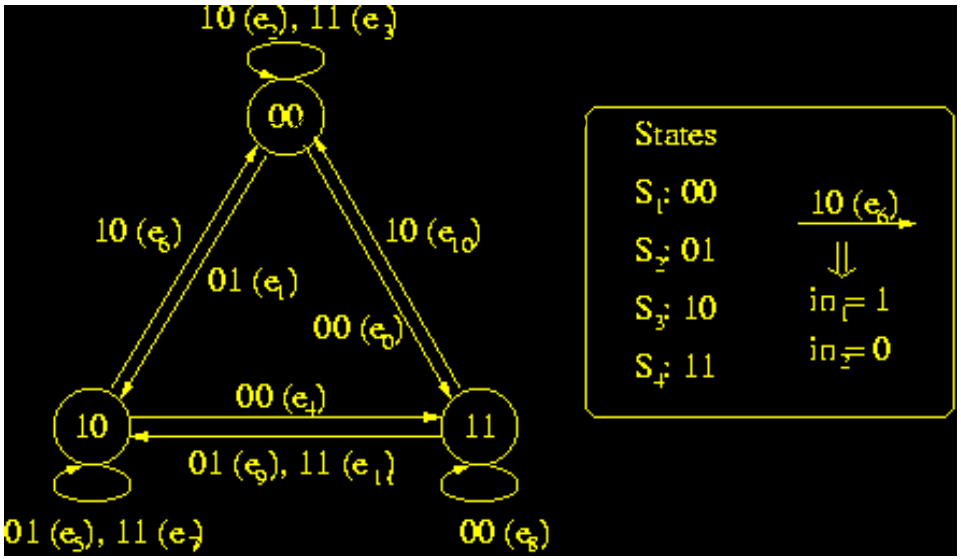
$$p_{x_i}^{1\to 0} = \lim_{N\to\infty} \frac{\sum_{j=1}^{NS} x_i(j)\overline{x_i(j+1)}}{NS}$$

$$p_{x_i}^{1\to 0} + p_{x_i}^{1\to 1} + p_{x_i}^{0\to 1} + p_{x_i}^{0\to 0} = 1$$

$$p_{x_i}^{1/0} = \frac{p_{x_i}^{0\to 1}}{p_{x_i}^{0\to 1} + p_{x_i}^{0\to 0}}$$

# State Transition Diagram Modeling



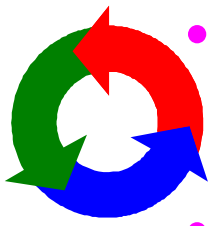




$$node_2(n+1) = (1 - x_1(n)) + x_1(n) \cdot x_2(n) \cdot node_2(n)$$

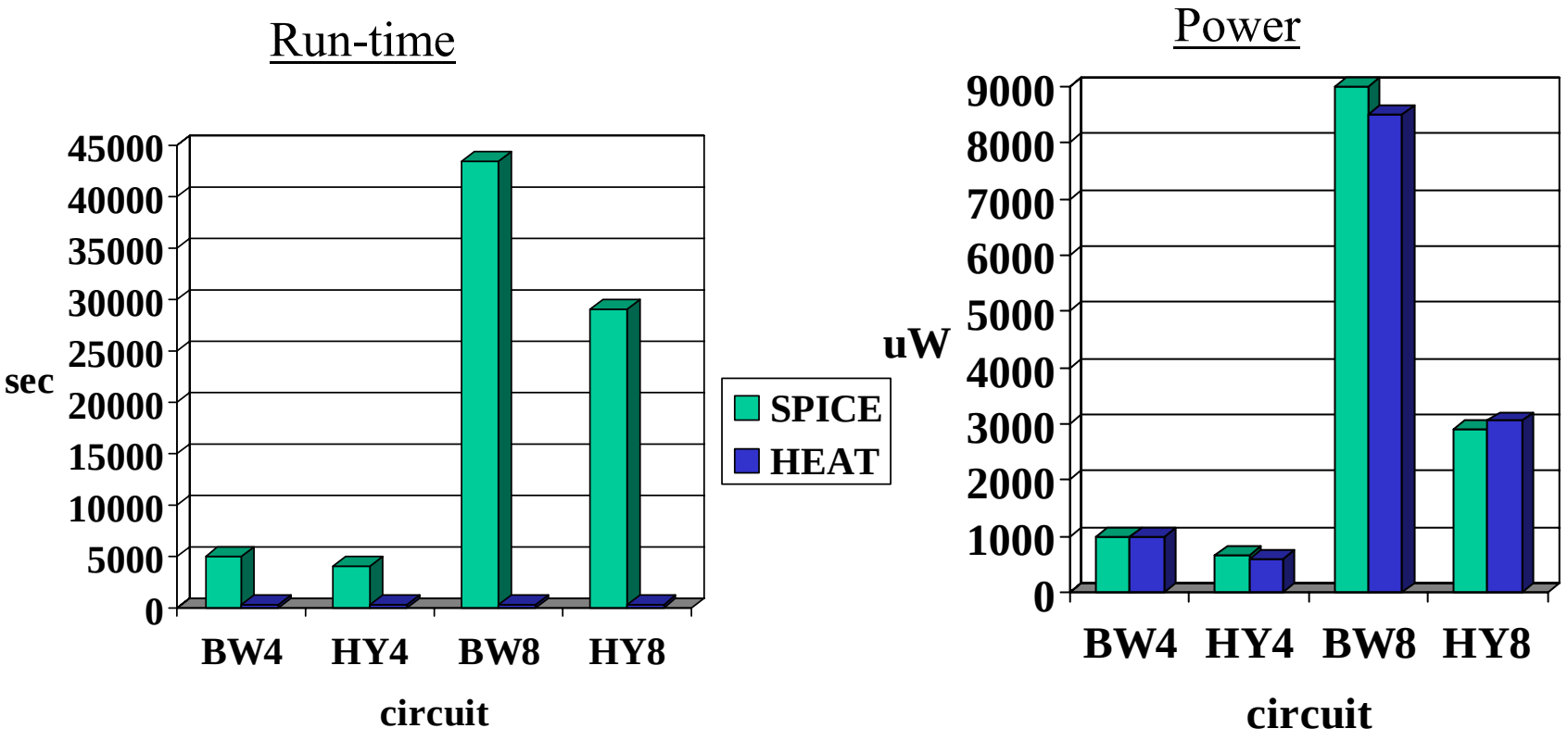
$$node_3(n+1) = (1 - x_1(n)) + (1 - x_2(n))$$

# The HEAT algorithm

- Partitioning of systems unit into smaller sub-units
- State transition diagram modeling
- Edge energy computation (HSPICE)
- Computation of steady-state probabilities (MATLAB)
- Edge activity computation
- Computation of average energy



# Performance Comparison




J. Satyanarayana and K.K. Parhi, "Power Estimation of Digital Datapaths using HEAT Tool", IEEE Design and Test Magazine, 17(2), pp. 101-110, April-June 2000

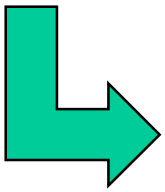
# Finite field arithmetic -- Addition and Multiplication

$$A = a_{m-1}\alpha^{m-1} + \ldots + a_1\alpha + a_0$$

$$B = b_{m-1}\alpha^{m-1} + \ldots + b_1\alpha + b_0$$

$$A + B = (a_{m-1} + b_{m-1})\alpha^{m-1} + \ldots + (a_1 + b_1)\alpha + (a_0 + b_0)$$

$$A \cdot B = (a_{m-1}\alpha^{m-1} + \ldots + a_1\alpha + a_0)(b_{m-1}\alpha^{m-1} + \ldots + b_1\alpha + b_0) \bmod (p(x))$$



Polynomial addition over GF(2)

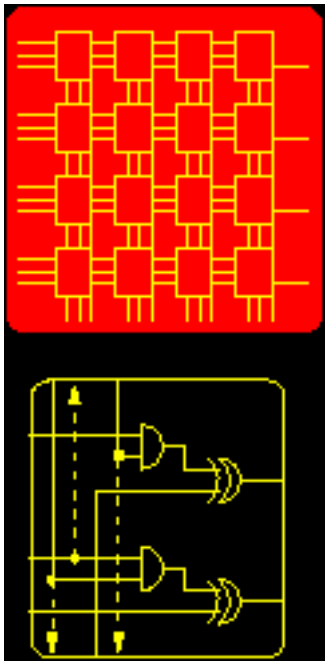
one's complement operation --> XOR gates

Polynomial multiplication and modulo operation

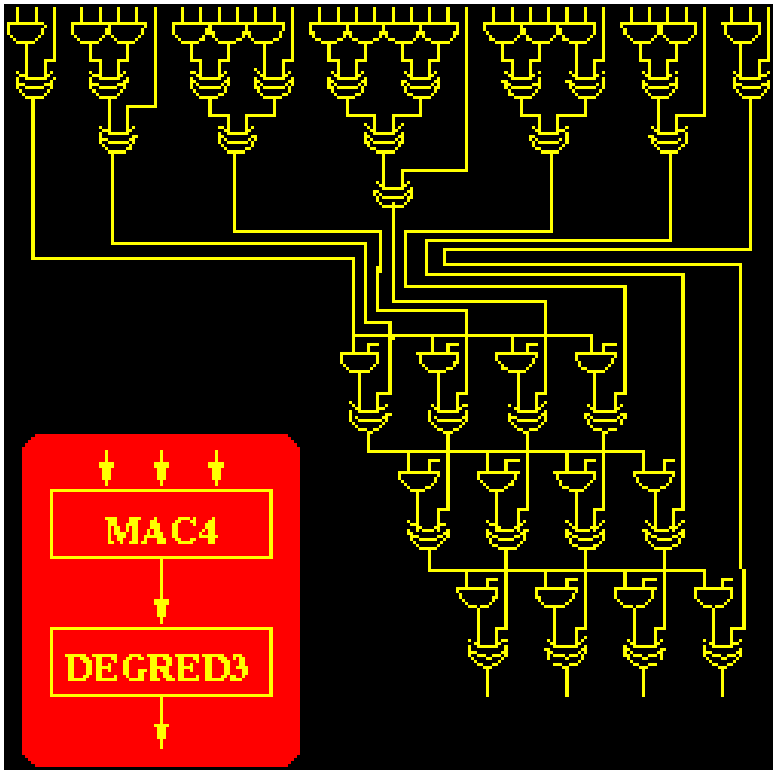
(modulo primitive polynomial p(x) )

# Programmable finite field multiplier

Array-type



Parallel




Digit-serial

MAC2
+
DEGRED2

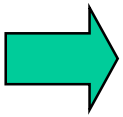
Four Instr.
- MAC2
- MAC2
- DEGRED2
- DEGRED2

# Finite field arithmetic-- programmable finite field multipliers

Programmability:-primitive polynomial p(x)
-field order m

How to achieve programmability:-control circuitry
-zero, pre & post padding

Polynomial multiplication
Polynomial modulo operation



Array-type multiplication
Fully parallel multiplication
Digit-serial/parallel multiplication

L. Song and K. K. Parhi, "Low-energy digit-serial/parallel finite field multipliers", Journal of VLSI Signal Processing, 19(2), pp. 149-166, June 1998

# Data-path architectures for low energy RS codecs

- Advantages of having two separate sub-arrays
  - Example: Vector-vector multiplication over GF($2^m$)

$$\begin{bmatrix} A_0 & A_1 & \dots A_{n-1} \end{bmatrix} \begin{bmatrix} B_0 \\ B_1 \\ \dots \\ B_{n-1} \end{bmatrix} = (A_0 B_0 + \dots + A_{n-1} B_{n-1}) \bmod (p(x))$$

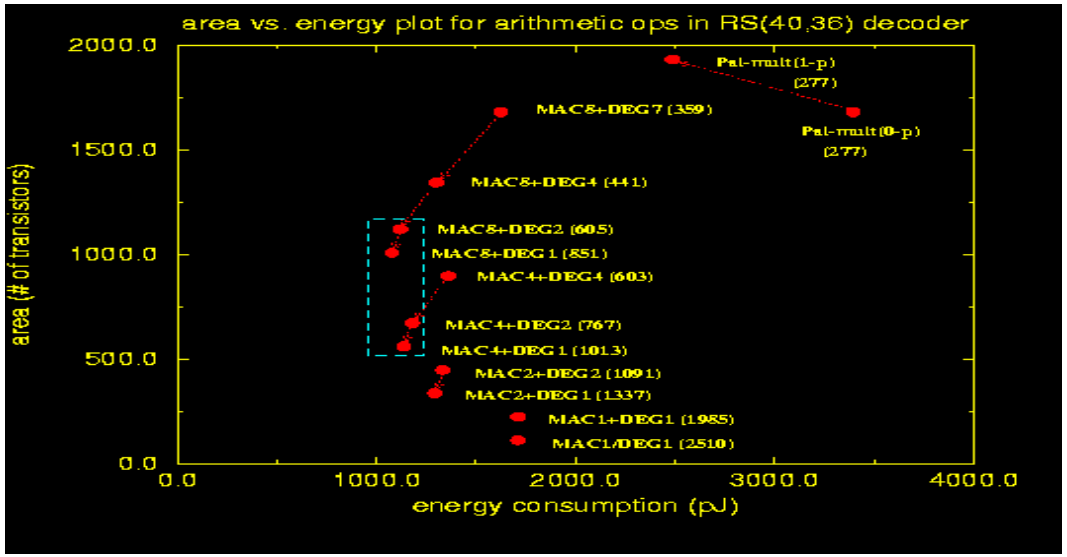
  - Assume energy(parallel multiplier)=Eng

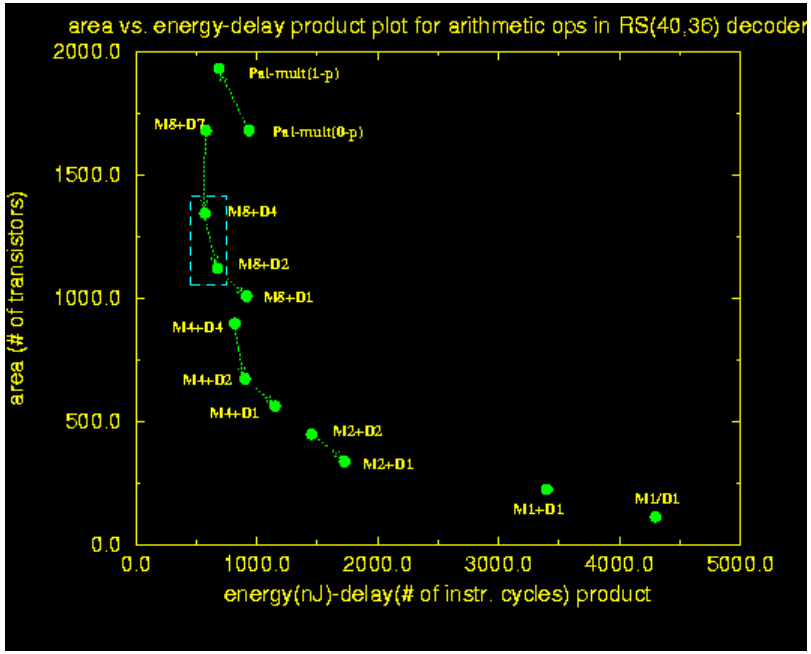
Energy(MAC8x8)=0.25 Eng
Energy(DEGRED7)=0.75 Eng

Total Energy(parallel)=Eng*n
Total Energy(MAC-D7)=0.25Eng*n+0.75Eng

$$s = \frac{Eng \cdot (n - (0.25n + 0.75))}{Eng \cdot n} \cong 75\%$$

# Data-path architectures for low-power RS encoder

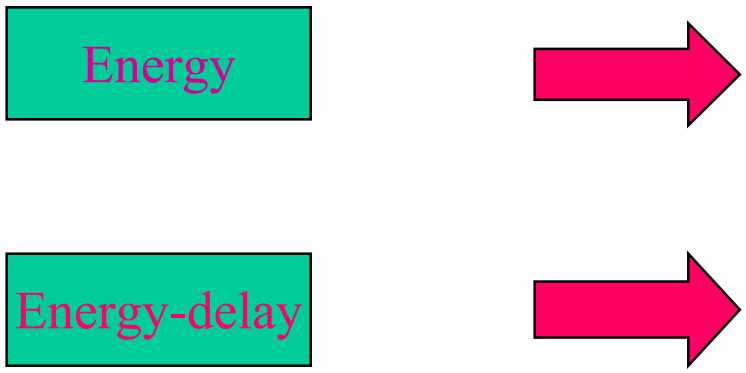



- Data-paths
  - One parallel finite field multiplier
  - Digit-serial multiplication: MACx and DEGREDy

# Data-path architectures for low energy RS codecs

- Data-path:
  - one parallel finite field multiplier
  - Digit-serial multiplication: MACx and DEGREDy




MAC8 + DEGRED2
MAC8 + DEGRED1
MAC4 + DEGRED2
MAC4 + DEGRED1

MAC8 + DEGRED4
MAC8 + DEGRED2

L. Song, K.K. Parhi, I. Kuroda, T. Nishitani, "Hardware/Software Codesign of Finite Field Datapath for Low-Energy Reed-Solomon Codecs", IEEE Trans. on VLSI Systems, 8(2), pp. 160-172, Apr. 2000

# Low power design challenges

- System Integration
- Application Specific architectures for Wireless/ADSL/Security
- Programmable DSPs to handle new application requirements
- Low-Power Architectures driven by Interconnect, Crosstalk in DSM technology
- How Far are we away from PDAs/Cell Phones for wireless video, internet access and e-commerce?