

In-depth Speed and Accuracy Comparison of Inductance Extraction for SoC Signal Integrity and Tool Integration

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The Outline for the presentation is:

1. SoC signal integrity issues
2. SoC design tools including inductance
3. In-depth studies of famous partial inductance formulae
4. PEEC-based 3-D field simulation
5. Reduced RLCK netlists for efficient SoC designs
6. Speed vs. accuracy comparisons
7. SoC signal integrity and tool integration
8. Conclusions and future work

The presentation reviews the trends that lead to the growing importance of inductance in real IC design today. Classical partial inductance solutions (Grover's Equation) are reviewed and compared.

An introduction is given to PEEC-based inductance calculation based on 3D field simulation. An efficient SoC design flow incorporating inductance effects is proposed and the various alternative calculation methods are benchmarked for speed and accuracy. Specifically the techniques are compared in their ability to deal with the skin-effect, eddy currents and the proximity effect.