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Expertise Area: System Architecture and Networking
Location: Ericsson, High-Tech Campus Eindhoven

Master Student Project

Title: Energy-aware buffer sizing for hard real-time streaming applications

Keywords

Data flow modeling and analysis, Buffer sizing, Voltage-frequency scaling

Problem Description

Dataflow (DF) is a well-known temporal analysis and programming model which is well suited to model concurrent real-time streaming applications. In dataflow, an application is modeled as a directed graph (DFG), where nodes (actors) represent processing elements and edges (queues with First-In-First-Out (FIFO) behavior) represent data dependencies. In Static Dataflow (StDF), actors have fixed execution times and they consume/produce fixed number of data items (tokens) from/on input/output edges. Moreover, StDF is equipped with techniques to verify real-time requirements such as deadlock-freedom and execution in bounded memory. In Dynamic Dataflow (DDF), actors may not have fixed execution times and fixed number of token consumptions/productions on edges. As a result, verifying real-time requirements for DDF may not be possible.

The computation of the minimum amount of memory needed by an application modeled as a data flow graph, to run without any deadlocks, is called buffer sizing. The problem of buffer sizing for real-time streaming applications, modeled as data-flow graphs, has been widely studied for various StDF flavors. One of the goals of the project is to extend the buffer sizing for Mode-Controlled Dataflow ([1], a restricted form of a DDF) which allows the same form of analysis as StDF.

Hard real-time streaming applications such as wireless transceivers, apart from having the real-time requirements, also have extremely low-energy processing requirements, as they typically run on battery-operated devices. Voltage and Frequency Scaling ([2], VFS) has been shown to be effective in reducing energy at system level by adjusting voltage and frequency, while meeting strict timing requirements.

The master thesis work is focused on studying the energy-aware buffer sizing for applications modeled as dataflow graphs i.e. to find a schedule that makes use of VFS to save energy, minimizes memory consumption through buffer sizing, while meeting strict timing requirements. The goals of your project are as follows:

- Extend the buffer sizing for Mode-Controlled Dataflow (MCDF).
- Investigate the effects of VFS on buffer sizing for MCDF.

References

[1]. O. Moreira, Temporal Analysis and Scheduling of Hard Real-Time Radios on a Multi-Processor. PhD thesis, TU/e, Eindhoven, NL, 2011.
[2]. P. Huang, et. al: Throughput-constrained voltage and frequency scaling for real-time heterogeneous multiprocessors. SAC 2013

The student is expected to have knowledge in:

- C, C++ and functional programming languages e.g. OCaml
- Embedded systems