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A framework for synthesis of reduced order models

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Abstract A framework for model reduction and synthesis is presented, which enables the re-use of reduced order models in circuit simulation. Especially when model reduction exploits structure preservation, we show that using the model as a current-driven element is possible, and allows for synthesis without controlled sources. Two synthesis techniques are considered: (1) by means of realizing the reduced transfer function into a netlist and (2) by unstamping the reduced system matrices into a circuit representation. The presented framework serves as a basis for reduction of large parasitic R/RC/RCL networks.

1 Introduction

The main motivation for this chapter comes from the need for a general framework for the (re)use of reduced order models in circuit simulation. Although many model order reduction methods have been developed and evolved since the 1990s (see for instance [1] for an overview), it is usually less clear how to use these methods efficiently in industrial practice, e.g., in a circuit simulator. One reason can be that the reduced order model does not satisfy certain physical properties, for instance, it may not be stable or passive while the original system is. Failing to preserve these properties is typically inherent to the reduced order method used (or its implementation). Passivity (and stability implicitly) can nowadays be preserved via several methods

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[19, 10, 21, 26, 2, 25, 16], but none address the practical aspect of (re)using the reduced order models with circuit simulation software (e.g., SPICE [9]). This brings forward another reason of concern within the circuit simulation industry. The linear circuit to be reduced is represented by a *netlist*, which is a description of the circuit element values (*R*,*L*,*C*) and their connections to the circuit nodes (see also Fig. 1). However, reduced order models (as a result of model reduction applied on the dynamical system describing the original circuit) are usually represented in terms of *system matrices* or of the *input-output transfer function*. Typically, circuit simulators are not prepared for inputs in a mathematical representation, and would require additional software architecture to handle them. In contrast, a reduced model in *netlist* representation could be easily coupled to bigger systems and directly simulated.

Synthesis is the realization step needed to map the reduced order model into a netlist consisting of electrical circuit components [13]. In [7] it was shown that passive systems (with positive real transfer functions) can be synthesized with positive *R*,*L*,*C* elements and transformers (see also [32]). Later developments [6] propose a method to circumvent the introduction of transformers, however the resulting realization is non-minimal (i.e., the number of electrical components generated during synthesis is too large). Allowing for possibly negative R, L, C values, other methods have been proposed via e.g. direct stamping [19, 18] or full realization [14, 20]. These mostly model the input/output connections of the reduced model with controlled sources.

In this chapter we consider two synthesis methods that do not involve controlled sources: (1) *Foster synthesis* [13], where the realization is done via the system's transfer function and (2) *RLCYSN synthesis by unstamping* [28], which exploits input-output structure preservation in the reduced system matrices [provided that the original system matrices are written in *modified nodal analysis (MNA)* representation]. The focus of this chapter is on structure preservation and RLCSYN, especially because synthesis by unstamping is simple to implement for both SISO and MIMO systems. Strengthening the result of [28], we give a simple procedure to reduce either current- or voltage-driven circuits directly in impedance form by removing all the sources. Such an impedance-based reduction enables synthesis without controlled sources. The reduced order model is available as a netlist, making it suitable for simulation and reuse in other designs. Similar software [8] is commercially available.

The material in this chapter is organized as follows. The remainder of this section introduces terminology for the different nodes pertaining to a circuit topology (Sect. 1.1). A brief mathematical formulation of model order reduction is given in Sect. 1.2. The Foster synthesis is presented in Sect. 2. In Sect. 3 we focus on reduction and synthesis with structure (and input/output) preservation. Sect. 3.1 describes the procedure to convert admittance models to impedance form, so that synthesized models are easily (re)used in simulation. Based on [28], Sect. 3.2 is an outline of SPRIM/IOPOR reduction and RLCSYN synthesis. Examples follow in Sect. 4, and Sect. 5 concludes.

1.1 Internal nodes, terminals, and ports

The terms internal nodes, terminals (or external nodes), and ports often occur in electronic engineering related papers. An *internal node* is a node in a circuit that is not visible on the outside of a circuit, i.e., no currents can be injected in an internal node (cf. node 1 in Figure 1). A *terminal (external node)* is a node that is visible on the outside, i.e., a node in which currents can be injected (cf. node a in Fig. 1). A port consists of two terminals that can be connected, for instance, by a source or another (sub)circuit (cf. port P in Fig. 1). Sometimes terminals are referred to as ports and vice versa: from the context it should then be clear which terminal(s) complete the ports; usually it is implicitly assumed that the ground node completes the ports. In Fig. 1, for instance, terminal a can be seen as a port (Q) by including the ground node.

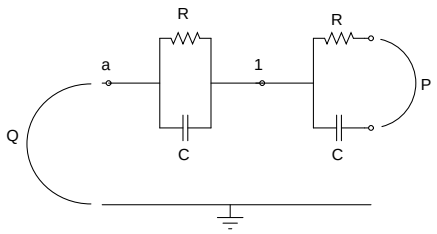

Fig. 1 Circuit with terminal a, internal node 1, port P, and port Q(a,0).

1.2 Problem formulation

In this chapter the dynamical systems $\Sigma(\mathbf{A},\mathbf{E},\mathbf{B},\mathbf{C},\mathbf{D})$ are of the form $\mathbf{E}\dot{\mathbf{x}}(t) = \mathbf{A}\mathbf{x}(t)+\mathbf{B}\mathbf{u}(t)$, $\mathbf{y}(t) = \mathbf{C}\mathbf{x}(t)+\mathbf{D}\mathbf{u}(t)$, where $\mathbf{A},\mathbf{E} \in \mathbb{R}^{n\times n}$, $\mathbf{E}$ may be singular but the pencil $(\mathbf{A},\mathbf{E})$ is regular, $\mathbf{B} \in \mathbb{R}^{n\times m}$, $\mathbf{C} \in \mathbb{R}^{p\times n}$, $\mathbf{x}(t) \in \mathbb{R}^n$, and $\mathbf{u}(t) \in \mathbb{R}^m$, $\mathbf{y}(t) \in \mathbb{R}^p$, $\mathbf{D} \in \mathbb{R}^{p\times m}$. If $m, p > 1$, the system is called multiple-input multiple-output (MIMO), otherwise it is called single-input single-output (SISO). The frequency domain transfer function is defined as: $\mathbf{H}(s) = \mathbf{C}(s\mathbf{E}-\mathbf{A})^{-1}\mathbf{B}+\mathbf{D}$. For systems in MNA form arising in circuit simulation see Sect. 3.

The model order reduction problem is to find, given an n-th order (descriptor) dynamical system, a k-th order system: $\widetilde{\mathbf{E}}\dot{\tilde{\mathbf{x}}}(t) = \widetilde{\mathbf{A}}\tilde{\mathbf{x}}(t)+\widetilde{\mathbf{B}}\mathbf{u}(t)$, $\tilde{\mathbf{y}}(t) = \widetilde{\mathbf{C}}\tilde{\mathbf{x}}(t)+\mathbf{D}\mathbf{u}(t)$ where $k < n$, and $\widetilde{\mathbf{E}},\widetilde{\mathbf{A}} \in \mathbb{R}^{k\times k}$, $\widetilde{\mathbf{B}} \in \mathbb{R}^{k\times m}$, $\widetilde{\mathbf{C}} \in \mathbb{R}^{p\times k}$, $\tilde{\mathbf{x}}(t) \in \mathbb{R}^k$, $\mathbf{u}(t) \in \mathbb{R}^m$, $\tilde{\mathbf{y}}(t) \in \mathbb{R}^p$, and $\mathbf{D} \in \mathbb{R}^{p\times m}$. The number of inputs and outputs is the same as for the original system, and the corresponding transfer function becomes: $\widetilde{\mathbf{H}}(s) = \widetilde{\mathbf{C}}(s\widetilde{\mathbf{E}}-\widetilde{\mathbf{A}})^{-1}\widetilde{\mathbf{B}}+\mathbf{D}$. For an overview of model order reduction methods, see [1, 5, 24]. Projection based model order reduction methods construct a reduced order model via Petrov-Galerkin projection:

$$\widetilde{\Sigma}(\widetilde{\mathbf{E}},\widetilde{\mathbf{A}},\widetilde{\mathbf{B}},\widetilde{\mathbf{C}},\mathbf{D}) \equiv (\mathbf{W}^*\mathbf{E}\mathbf{V},\mathbf{W}^*\mathbf{A}\mathbf{V},\mathbf{W}^*\mathbf{B},\mathbf{C}\mathbf{V},\mathbf{D}), \tag{1}$$

where $\mathbf{V},\mathbf{W} \in \mathbb{R}^{n\times k}$ are matrices whose $k < n$ columns form bases for relevant subspaces of the state-space. There are several projection methods, that differ in the way the matrices $\mathbf{V}$ and $\mathbf{W}$ are chosen. These also determine which properties are preserved after reduction. Some stability preserving methods are: *modal approximation* [23], *poor man's TBR* [22]. Among *moment matching* [11] methods, the following preserve passivity: *PRIMA* [19], *SPRIM* [10], *spectral zero interpolation*, [2, 25, 16, 30]. From the balancing methods, *balanced truncation* [4] preserves stability, and *positive real balanced truncation* [21, 26] preserves passivity.

2 Foster synthesis of rational transfer functions

This section describes the Foster synthesis method, which was developed in the 1930s by Foster and Cauer [13] and involves realization based on the system's transfer function. The Foster approach can be used to realize any reduced order model that is computed by standard projection based model order reduction techniques. Realizations will be described in terms of SISO impedances (Z-parameters). For equivalent realizations in terms of admittances (Y-parameters), see for instance [13, 27]. Given the reduced system (1) and assuming that all its finite poles are simple [i.e., the matrix pencil $(\widetilde{\mathbf{A}},\widetilde{\mathbf{E}})$ is non-defective], consider the partial fraction expansion [17] of its transfer function:

$$\widetilde{\mathbf{H}}(s) = \sum_{i=1}^{k} \frac{\tilde{r}_i}{s-\tilde{p}_i} + \mathbf{D}, \tag{2}$$

The residues are $\tilde{r}_i = \frac{(\widetilde{\mathbf{C}}\tilde{\mathbf{x}}_i)(\tilde{\mathbf{y}}_i^*\widetilde{\mathbf{B}})}{\tilde{\mathbf{y}}_i^*\widetilde{\mathbf{E}}\tilde{\mathbf{x}}_i}$, the poles are $\tilde{p}_i$ and, if non-zero, $\mathbf{D}$ gives additional contribution from poles at ∞. An eigentriplet $(\tilde{p}_i,\tilde{\mathbf{x}}_i,\tilde{\mathbf{y}}_i)$ is composed of an eigenvalue $\tilde{p}_i$ of $(\widetilde{\mathbf{A}},\widetilde{\mathbf{E}})$ and the corresponding right and left eigenvectors $\tilde{\mathbf{x}}_i,\tilde{\mathbf{y}}_i \in \mathbb{C}^k$. The expansion (2) consists of basic summands of the form:

$$Z(s) = r_1 + \frac{r_2}{s-p_2} + \frac{r_3}{s} + \left(\frac{r_4}{s-p_4} + \frac{\bar{r}_4}{s-\bar{p}_4}\right) + sr_6 + \left(\frac{r_7}{s-p_7} + \frac{r_7}{s-\bar{p}_7}\right), \tag{3}$$

where for completeness we can assume that any kind of poles may appear, i.e., either purely real, purely imaginary, in complex conjugate pairs, at ∞ or at 0 (see also Table 1). The Foster realization converts each term in (3) into the corresponding circuit block with R,L,C components, and connects these blocks in series in the final netlist. This is shown in Fig. 2. Note that any reordering of the circuit blocks in the realization of (3) in Fig. 2 still is a realization of (3). The values for the circuit components in Fig. 2 are determined according to Table 1.

The realization in netlist form can be implemented in any language such as SPICE [9], so that it can be reused and combined with other circuits as well. The advantages of Foster synthesis are: (1) its straightforward implementation for single-input-single-output (SISO) transfer functions, via either the impedance or the admittance transfer function, (2) after reducing purely *RC* or *RL* circuits via modal ap-

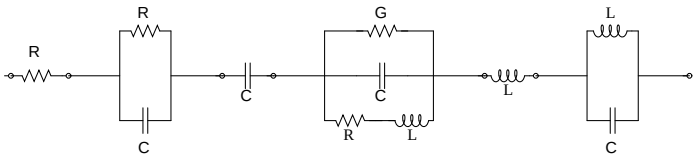

Fig. 2 Realization of a general impedance transfer function as a series *RLC* circuit.

Table 1 Circuit element values for Fig. 2 for the Foster impedance realization of (3)

pole	residue	R(Ohm)	C(F)	L(H)	G(Ohm$^-$1)
$p_1 = \infty$	$r_1 \in \mathbb{R}$	r_1			
$p_2 \in \mathbb{R}$	$r_2 \in \mathbb{R}$	$-\frac{r_2}{p_2}$	$\frac{1}{r_2}$		
$p_3 = 0$	$r_3 \in \mathbb{R}$		$\frac{1}{r_3}$		
$p_4 = \sigma + i\omega \in \mathbb{C}$	$r_4 = \alpha + i\beta \in \mathbb{C}$	$\frac{a_0}{a_1}L$	$\frac{1}{a_1}$	$\frac{a_1^3}{a_1^2 b_0 - a_0(a_1 b_1 - a_0)}$	$\frac{a_1 b_1 - a_0}{a_1^2}$
$p_5 \equiv \bar{p}_4$	$r_5 \equiv \bar{r}_4$				
$a_0 = -2(\alpha\sigma + \beta\omega), \quad a_1 = 2\alpha, \quad b_0 = \sigma^2 + \omega^2, \quad b_1 = -2\sigma$					
$p_6 = \infty$	$r_6 \in \mathbb{R}$			r_6	
$p_7 \in i\mathbb{R}$	$r_7 \in \mathbb{R}$		$\frac{1}{r_7}$	$\frac{2r_7}{p_7 p_7}$	
$p_8 \equiv \bar{p}_7$	$r_8 \equiv \bar{r}_7$				

proximation [23], the reduced netlists obtained from Foster synthesis are guaranteed to have positive *RC* or *RL* values respectively (see [15] for a proof). Note however that Foster synthesis does not guarantee positive circuit elements in general (e.g., when used to synthesize reduced models originating from *RLC* circuits, or reduced models of *RC* and *RL* circuits that were obtained with methods different than modal approximation). The main disadvantage is that for multi-input-multi-output transfer functions, finding the Foster realization (see for instance [27]) is cumbersome and may also give dense reduced netlists (i.e., all nodes are interconnected). This is because the Foster synthesis of a k-dimensional reduced system with p terminals, will generally yield $O(p^2k)$ circuit elements.

3 Structure preservation and synthesis by unstamping

This section describes the second synthesis approach, which is based on *unstamping* the reduced matrix data into an *RLC* netlist and is denoted by RLCSYN [28]. It is suitable for obtaining netlist representations for models reduced via methods that preserve the MNA structure and the input-output connectivity at the circuit terminals, such as the *input-output structure preserving* method SPRIM/IOPOR[28]. The strength of the result in [28] is that the input/output connectivity is synthesized after reduction without controlled sources, provided that the system is in *impedance form* (i.e., inputs are currents injected into the circuit terminals, and outputs are voltages measured at the terminals). For ease of understanding, the input-output structure preserving reduction from [28] can be interpreted as model reduction with *preservation of external nodes* [e.g., after reducing the circuit in Fig. 1, the nodes forming

ports Q and P are external (terminals) and will also appear in the synthesized reduced model]. This way the reduced netlist can be easily coupled to other circuitry in place of the original netlist, and (re)using the reduced model in simulation becomes straightforward. The main drawback is that, when the reduced system matrices are dense and the number of terminals is large [$O(10^3)$], the netlist obtained from RLCSYN will be dense. For a k dimensional reduced network with p terminals, the RLCSYN synthesized netlist will generally have $O(p^2k^2)$ circuit elements. The density of the reduced netlist however is not a result of the synthesis procedure, but a consequence of the fact that the reduced system matrices are dense. Developments for sparsity preserving model reduction for multi-terminal circuits can be found in [29], where sparse netlists are obtained by synthesizing sparse reduced models via RLCSYN.

First, we motivate reduction and synthesis in impedance form, and show how it also applies for systems that are originally in admittance form. Then we explain model reduction via SPRIM/IOPOR, followed by RLCSYN synthesis.

3.1 A simple admittance to impedance conversion

In [28] it was shown how SPRIM/IOPOR preserves the structure of the input/output connectivity when the original model is in impedance form, allowing for synthesis via RLCSYN without controlled sources. The emerging question is: how to ensure synthesis without controlled sources, if the original model is in admittance form (i.e., it is voltage driven)? We show that reduction and synthesis via the input impedance transfer function is possible by removing any voltage sources from the original circuit a priori and re-inserting them in the reduced netlist if needed.

Consider the modified nodal analysis (MNA) description of an input *admittance*[1] type *RLC* circuit, driven by n_s voltage sources:

$$\underbrace{\begin{pmatrix} \mathscr{C} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathscr{L} \end{pmatrix}}_{\mathbf{E}_Y} \underbrace{\frac{d}{dt}\begin{pmatrix} \mathbf{v}(t) \\ \mathbf{i}_S(t) \\ \mathbf{i}_L(t) \end{pmatrix}}_{\dot{\mathbf{x}}_Y} + \underbrace{\begin{pmatrix} \mathscr{G} & \mathscr{E}_\mathbf{v} & \mathscr{E}_\mathbf{I} \\ -\mathscr{E}_\mathbf{v}^* & \mathbf{0} & \mathbf{0} \\ -\mathscr{E}_\mathbf{I}^* & \mathbf{0} & \mathbf{0} \end{pmatrix}}_{-\mathbf{A}_Y} \underbrace{\begin{pmatrix} \mathbf{v}(t) \\ \mathbf{i}_S(t) \\ \mathbf{i}_L(t) \end{pmatrix}}_{\mathbf{x}_Y} = \underbrace{\begin{pmatrix} \mathbf{0} \\ \mathscr{B} \\ \mathbf{0} \end{pmatrix}}_{\mathbf{B}_Y} \mathbf{u}(t), \qquad (4)$$

where $\mathbf{u}(t) \in \mathbb{R}^{n_s}$ are input voltages and $\mathbf{y}(t) = \mathbf{C}_Y\mathbf{x}(t) \in \mathbb{R}^{n_s}$ are output currents, $\mathbf{C}_Y = \mathbf{B}_Y^*$. The states are $\mathbf{x}_Y(t)^T = [\mathbf{v}(t),\ \mathbf{i}_S(t),\ \mathbf{i}_L(t)]^T$, with $\mathbf{v}(t) \in \mathbb{R}^{n_v}$ the node voltages, $\mathbf{i}_S(t) \in \mathbb{R}^{n_s}$ the currents through the voltage sources, and $\mathbf{i}_L(t) \in \mathbb{R}^{n_l}$ the currents through the inductors, $n_v + n_s + n_l = n$. The $n_v = n_1 + n_2$ node voltages are formed by the n_1 external nodes/terminals[2] and the n_2 internal nodes (assuming that

[1] The subscript Y refers to quantities associated with a system in admittance form.

[2] The MNA form (4) corresponds to the ungrounded circuit (i.e., the reference node is counted within the n_1 external nodes), resulting in a defective matrix pencil $(\mathbf{A}_Y, \mathbf{E}_Y)$. For subsequent computations such as the construction of a Krylov subspace, the pencil $(\mathbf{A}_Y, \mathbf{E}_Y)$ must be regular. Thus in (4), one node must be chosen as a ground (reference) node by removing the row/column corresponding to that node; this ensures that the regularity conditions (i) and (ii) from [32, page 5, Assumption 4] are satisfied. The positive definiteness of $\mathscr{C}, \mathscr{L}, \mathscr{G}$ is also a necessary condition to ensure the circuit's passivity.

the voltage sources may be ungrounded, n_1 satisfies: $n_s < n_1 \leq 2n_s+1$). The dimensions of the underlying matrices are: $\mathscr{C} \in \mathbb{C}^{n_v \times n_v}$, $\mathscr{G} \in \mathbb{C}^{n_v \times n_v}$, $\mathscr{E}_v \in \mathbb{C}^{n_v \times n_s}$, $\mathscr{L} \in \mathbb{C}^{n_l \times n_l}$, $\mathscr{E}_l \in \mathbb{C}^{n_v \times n_l}$, $\mathscr{B} \in \mathbb{C}^{n_1 \times n_s}$. Assuming without loss of generality that (4) is permuted such that the *first* n_1 nodes are the external nodes, the input voltages are determined by a linear combination of $\mathbf{v}_{1:n_1}(t)$ only. Thus the following holds:

$$\mathscr{E}_{\mathbf{v}} = \begin{pmatrix} \mathscr{B}_v \\ \mathbf{0}_{n_2 \times n_s} \end{pmatrix} \in \mathbb{C}^{n_v \times n_s}, \;\; \mathscr{B}_v \in \mathbb{C}^{n_1 \times n_s}, \;\; \mathscr{B} = -\mathscr{B}_v. \tag{5}$$

We derive the first order impedance-type system associated with (4). Note that by definition, $\mathbf{i}_S(t)$ flows **out of** the circuit terminals into the voltage source (i.e., from the $+$ to the $-$ terminal of the voltage source, see also [19, Figure 3] [15]). We can define new input currents as the currents flowing **into** the circuit terminals: $\mathbf{i}_{in}(t) = -\mathbf{i}_S(t)$. Since $\mathbf{v}_{1:n_1}(t)$ are the terminal voltages, they describe the new output equations, and it is straightforward to rewrite (4) in the impedance form:

$$\begin{cases} \underbrace{\begin{pmatrix} \mathscr{C} & \mathbf{0} \\ \mathbf{0} & \mathscr{L} \end{pmatrix}}_{\mathbf{E}} \underbrace{\frac{d}{dt}\begin{pmatrix} \mathbf{v}(t) \\ \mathbf{i}_L(t) \end{pmatrix}}_{\dot{\mathbf{x}}} + \underbrace{\begin{pmatrix} \mathscr{G} & \mathscr{E}_{\mathbf{l}} \\ -\mathscr{E}_{\mathbf{l}}^* & \mathbf{0} \end{pmatrix}}_{-\mathbf{A}} \underbrace{\begin{pmatrix} \mathbf{v}(t) \\ \mathbf{i}_L(t) \end{pmatrix}}_{\mathbf{x}} = \underbrace{\begin{pmatrix} \mathscr{E}_{\mathbf{v}} \\ \mathbf{0} \end{pmatrix}}_{\mathbf{B}} \mathbf{i}_{in}(t) \\ \underbrace{\begin{pmatrix} \mathscr{E}_v^* & \mathbf{0} \end{pmatrix}}_{\mathbf{C}} \underbrace{\begin{pmatrix} \mathbf{v}(t) \\ \mathbf{i}_L(t) \end{pmatrix}}_{\mathbf{x}} = \mathbf{y}(t) \;=\; \mathscr{B}_v \mathbf{v}_{1:n_1}(t), \quad \mathscr{E}_v^* = \begin{pmatrix} \mathscr{B}_v^* & \mathbf{0}_{n_s \times n_2} \end{pmatrix} \end{cases} \tag{6}$$

where $\mathbf{B}$ describes the new *input incidence matrix* corresponding the input currents, $\mathbf{i}_{in}$. The new *output incidence matrix* is $\mathbf{C}$, corresponding to the voltage drops over the circuit terminals. We emphasize that (6) has fewer unknowns than (4), since the currents $\mathbf{i}_S$ have been eliminated. The transfer function associated to (6) is an input impedance: $\mathbf{H}(s) = \frac{\mathbf{y}(s)}{\mathbf{i}_{in}(s)}$. In Sect. 3.2 we explain how to obtain an impedance type reduced order model in the input/output structure preserved form:

$$\begin{cases} \underbrace{\begin{pmatrix} \widetilde{\mathscr{C}} & \mathbf{0} \\ \mathbf{0} & \widetilde{\mathscr{L}} \end{pmatrix}}_{\widetilde{\mathbf{E}}} \underbrace{\frac{d}{dt}\begin{pmatrix} \widetilde{\mathbf{v}}(t) \\ \widetilde{\mathbf{i}}_L(t) \end{pmatrix}}_{\dot{\widetilde{\mathbf{x}}}} + \underbrace{\begin{pmatrix} \widetilde{\mathscr{G}} & \widetilde{\mathscr{E}}_l \\ -\widetilde{\mathscr{E}}_l^* & \mathbf{0} \end{pmatrix}}_{-\widetilde{\mathbf{A}}} \underbrace{\begin{pmatrix} \widetilde{\mathbf{v}}(t) \\ \widetilde{\mathbf{i}}_L(t) \end{pmatrix}}_{\widetilde{\mathbf{x}}} = \underbrace{\begin{pmatrix} \widetilde{\mathscr{E}}_v \\ \mathbf{0} \end{pmatrix}}_{\widetilde{\mathbf{B}}} \mathbf{i}_{in}(t) \\ \underbrace{\begin{pmatrix} \widetilde{\mathscr{E}}_v^* & \mathbf{0} \end{pmatrix}}_{\widetilde{\mathbf{C}}} \underbrace{\begin{pmatrix} \widetilde{\mathbf{v}}(t) \\ \widetilde{\mathbf{i}}_L(t) \end{pmatrix}}_{\widetilde{\mathbf{x}}} = \mathbf{y}(t) \;=\; \mathscr{B}_v \mathbf{v}_{1:n_1}(t), \;\; \tilde{\mathscr{E}}_v^* = \begin{pmatrix} \mathscr{B}_v^* & \mathbf{0}_{n_s \times k_2} \end{pmatrix} \end{cases} \tag{7}$$

where $\widetilde{\mathscr{C}}, \widetilde{\mathscr{L}}, \widetilde{\mathscr{G}}, \widetilde{\mathscr{E}}_v$ are the reduced MNA matrices, and the reduced input impedance transfer function is: $\widetilde{\mathbf{H}}(s) = \frac{\widetilde{\mathbf{y}}(s)}{\mathbf{i}_{in}(s)}$. Due to the input/output preservation, the circuit terminals are easily preserved in the reduced model (7). The simple example in Sect. 4.1 illustrates the procedure just described.

It turns out that after reduction and synthesis, the reduced model (7) can still be used as a voltage driven admittance block in simulation. This is shown next. We can

rewrite the second equation in (7) as: $\left(-\widetilde{\mathscr{E}}_v^* \; \mathbf{0} \; \mathbf{0}\right)\left(\widetilde{\mathbf{v}}(t)^T \; \widetilde{\mathbf{i}}_S(t)^T \; \widetilde{\mathbf{i}}_L(t)^T\right)^T = \mathscr{B}\mathbf{u}(t)$. This result together with $\mathbf{i}_{in}(t) = -\mathbf{i}_S(t)$, reveals that (7) can be rewritten as:

$$\underbrace{\begin{pmatrix}\widetilde{\mathscr{C}} & \mathbf{0} & \mathbf{0}\\ \mathbf{0} & \mathbf{0} & \mathbf{0}\\ \mathbf{0} & \mathbf{0} & \widetilde{\mathscr{L}}\end{pmatrix}}_{\widetilde{\mathbf{E}}_Y}\underbrace{\frac{d}{dt}\begin{pmatrix}\widetilde{\mathbf{v}}(t)\\ \mathbf{i}_S(t)\\ \widetilde{\mathbf{i}}_L(t)\end{pmatrix}}_{\dot{\widetilde{\mathbf{x}}}_Y} + \underbrace{\begin{pmatrix}\widetilde{\mathscr{G}} & \widetilde{\mathscr{E}}_v & \widetilde{\mathscr{E}}_l\\ -\widetilde{\mathscr{E}}_v^* & \mathbf{0} & \mathbf{0}\\ -\widetilde{\mathscr{E}}_l^* & \mathbf{0} & \mathbf{0}\end{pmatrix}}_{-\widetilde{\mathbf{A}}_Y}\underbrace{\begin{pmatrix}\widetilde{\mathbf{v}}(t)\\ \mathbf{i}_S(t)\\ \widetilde{\mathbf{i}}_L(t)\end{pmatrix}}_{\widetilde{\mathbf{x}}_Y} = \underbrace{\begin{pmatrix}\mathbf{0}\\ \mathscr{B}\\ \mathbf{0}\end{pmatrix}}_{\widetilde{\mathbf{B}}_Y}\mathbf{u}(t), \tag{8}$$

which has the same structure as the original admittance model (4). Conceptually one could have reduced system (4) directly via the input admittance. In that case, synthesis by unstamping via RLCSYN [28] would have required controlled sources [14]. As shown above, this is avoided by: applying the simple admittance-to-impedance conversion (4) to (6), reducing (6) to (7), and finally reinserting voltage sources after synthesis [if the input-output structure preserved admittance reduced admittance (8) is needed]. Being only a pre- and post-processing step, the proposed voltage-source removal and re-insertion can be applied irrespective of the model reduction algorithm used. For ease of understanding we relate it here to model reduction via SPRIM/IOPOR.

3.2 I/O structure preserving reduction and RLCSYN synthesis

The reduced input impedance model (7) is obtained via the input-output structure preserving SPRIM/IOPOR projection [28] as follows. Let $\mathbf{V} = \left(\mathbf{V}_1^T, \mathbf{V}_2^T, \mathbf{V}_3^T\right)^T \in \mathbb{C}^{((n_1+n_2+n_l)\times k)}$ be the projection matrix obtained with PRIMA [19], where $\mathbf{V}_1 \in \mathbb{C}^{(n_1\times k)}$, $\mathbf{V}_2 \in \mathbb{C}^{(n_2\times k)}$, $\mathbf{V}_3 \in \mathbb{C}^{(n_l\times k)}$, $k \geq n_1$, $i = 1\ldots 3$. After appropriate orthonormalization (e.g., via Modified Gram-Schmidt [23, Chapter 1]), we obtain: $\widetilde{\mathbf{V}}_i = \text{orth}(\mathbf{V}_i) \in \mathbb{C}^{n_i\times k_i}$,$k_i \leq k$. The SPRIM [10] block structure preserving projection is: $\widetilde{\mathbf{V}} = \text{blkdiag}\left(\widetilde{\mathbf{V}}_1, \widetilde{\mathbf{V}}_2, \widetilde{\mathbf{V}}_3\right) \in \mathbb{C}^{n\times(k_1+k_2+k_3)}$, which does not yet preserve the structure of the input and output matrices. The input-output structure preserving SPRIM/IOPOR [28] projection is $\widetilde{\mathbf{W}} = \begin{pmatrix}\mathbf{W} & \mathbf{0}\\ \mathbf{0} & \widetilde{\mathbf{V}}_3\end{pmatrix} \in \mathbb{C}^{n\times(n_1+k_2+k_3)}$ where:

$$\mathbf{W} = \begin{pmatrix}\mathbf{I}_{n_1\times n_1} & \mathbf{0}\\ \mathbf{0} & \widetilde{\mathbf{V}}_2\end{pmatrix} \in \mathbb{C}^{(n_1+n_2)\times(n_1+k_2)}. \tag{9}$$

Recalling (5), we obtain the reduced system matrices in (7): $\widetilde{\mathscr{C}} = \mathbf{W}^*\mathscr{C}\mathbf{W}$, $\widetilde{\mathscr{G}} = \mathbf{W}^*\mathscr{G}\mathbf{W}$, $\widetilde{\mathscr{L}} = \widetilde{\mathbf{V}}_3^*\mathscr{L}\widetilde{\mathbf{V}}_3$, $\widetilde{\mathscr{E}}_l = \mathbf{W}^*\mathscr{E}_l\widetilde{\mathbf{V}}_3$, $\widetilde{\mathscr{E}}_v = \mathbf{W}^*\mathscr{E}_\mathbf{v} = \left(\mathscr{B}_v^* \; \mathbf{0}_{n_s\times k_2}\right)^*$, which compared to (5) clearly preserve input-output structure. Therefore a netlist representation for the reduced impedance-type model can be obtained, that is driven injected currents just as the original circuit. This is done via the RLCSYN [28] unstamping procedure. To this end, we use the Laplace transform and convert (7) to the second order form:

$$\begin{cases} [s\widetilde{\mathscr{C}}+\widetilde{\mathscr{G}}+\frac{1}{s}\widetilde{\Gamma}]\widetilde{\mathbf{v}}(s)=\widetilde{\mathscr{E}}_{\mathbf{v}}\mathbf{i}_{in}(s) \\ \widetilde{\mathbf{y}}(s)=\widetilde{\mathscr{E}}_{v}^{*}\widetilde{\mathbf{v}}(s), \end{cases} \tag{10}$$

where $\widetilde{\mathbf{i}}_L(s)=\frac{1}{s}\widetilde{\mathscr{L}}^{-1}\left(\widetilde{\mathscr{E}}_{\mathbf{l}}^{*}\right)\widetilde{\mathbf{v}}(s)$ and $\widetilde{\Gamma}=\widetilde{\mathscr{E}}_{l}\widetilde{\mathscr{L}}^{-1}\widetilde{\mathscr{E}}_{l}^{*}$.

The presentation of RLCSYN follows [28, Sect. 4], [15] and is only summarized here. In circuit simulation, the process of forming the $\mathscr{C},\mathscr{G},\mathscr{L}$ system matrices from the individual branch element values is called "stamping". The reverse operation of "unstamping" involves decomposing entry-wise the values of the reduced system matrices in (10) into the corresponding *R*, *L*, and *C* values. When applied on reduced models, the unstamping procedure may produce negative circuit elements because the reduced system matrices are no longer diagonally dominant (while the original matrices were). Obtaining positive circuit elements only is subject to further research. The resulting *R*s, *L*s and *C*s are connected in the reduced netlist according to the MNA topology. The reduced input/output matrices of (10) directly reveal the input connections in the reduced model via injected currents, without any controlling elements. The prerequisites for an unstamping realization procedure therefore are:

1. The original system is in MNA impedance form (6). If the system is of admittance type (4), apply the admittance-to-impedance conversion from Sect. 3.1.
2. In (6), no *L*s are directly connected to the input terminals so that, after reduction, diagonalization and regularization preserve the input/output structure.
3. System (6) is reduced with SPRIM/IOPOR [28] to (7) and converted to second order form (10). The alternative is to obtain the second order form of the original system first, and reduce it directly with SAPOR/IOPOR [28, 3].
4. The reduced system (10) must be diagonalized and regularized according to [28]. Diagonalization ensures that all inductors in the synthesized model are connected to ground (i.e., there are no inductor loops). Regularization eliminates spurious over-large inductors. These steps however are not needed for purely *RC* circuits.

4 Numerical examples

We apply the proposed reduction and synthesis framework on several test cases. The first is a simple circuit which illustrates the complete admittance-to-impedance formulation and the RLCSYN unstampting procedure, as described in Sect. 3. The second example is a single-input-single-output (SISO) transmission line model, while the third is a multi-input-multi-output (MIMO) model of a spiral inductor. For the SISO example, one can easily provide synthesized models via both Foster and RLCSYN. For the MIMO example, a synthesized model can be obtained straightforwardly with RLCSYN, thus RLCSYN synthesis is preferred over Foster synthesis.

4.1 Illustrative example

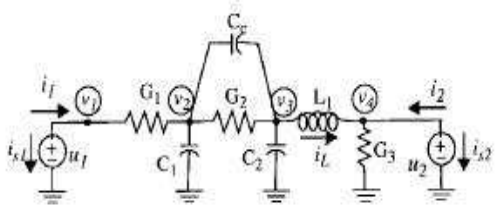

Fig. 3 Admittance-type circuit driven by input voltages [19]. $G_{1,2,3} = 0.1S$, $L_1 = 10^{-3}H$, $C_{1,2} = 10^{-6}$, $C_c = 10^{-4}$, $\|u_{1,2}\| = 1$.

The circuit in Fig. 3 is voltage driven, and the MNA admittance form (4) is:

$$\left(\begin{array}{cccc|c|c} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & C_1+C_c & -C_c & 0 & 0 \\ 0 & 0 & -C_c & C_2+C_c & 0 & 0 \\ \hline 0 & 0 & 0 & 0 & 0 & 0 \\ \hline 0 & 0 & 0 & 0 & 0 & 0 \\ \hline 0 & 0 & 0 & 0 & 0 & L \end{array}\right) \left(\begin{array}{c} \dot{v}_1 \\ \dot{v}_4 \\ \dot{v}_2 \\ \dot{v}_3 \\ \hline \dot{i}_{S_1} \\ \dot{i}_{S_2} \\ \hline \dot{i}_L \end{array}\right) + \left(\begin{array}{cccc|c|c} G_1 & 0 & -G_1 & 0 & 1 & 0 \\ 0 & G_3 & 0 & 0 & 0 & 1 \\ -G_1 & 0 & G_1+G_2 & -G_2 & 0 & 0 \\ 0 & 0 & -G_2 & G_2 & 0 & 1 \\ \hline -1 & 0 & 0 & 0 & 0 & 0 \\ \hline 0 & -1 & 0 & 0 & 0 & 0 \\ \hline 0 & 1 & 0 & -1 & 0 & 0 \end{array}\right) \left(\begin{array}{c} v_1 \\ v_4 \\ v_2 \\ v_3 \\ \hline i_{S_1} \\ i_{S_2} \\ \hline i_L \end{array}\right) = \left(\begin{array}{cc} 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ \hline -1 & 0 \\ 0 & -1 \\ \hline 0 & 0 \end{array}\right) \begin{pmatrix} u_1 \\ u_2 \end{pmatrix} \tag{11}$$

Notice that

$$\mathbf{i}_{in} = \begin{pmatrix} i_1 \\ i_2 \end{pmatrix} = -\begin{pmatrix} i_{S_1} \\ i_{S_2} \end{pmatrix} \tag{12}$$

$$\mathbf{u} = \begin{pmatrix} u_1 \\ u_2 \end{pmatrix} = \begin{pmatrix} v_1 \\ v_4 \end{pmatrix}, \tag{13}$$

thus the external nodes (input nodes/terminals) are v_1 and v_4, and the internal nodes are v_2 and v_3. As described in Sect. 3.1, (11) has an equivalent impedance formulation (6), with:

$$\mathscr{C} = \begin{pmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & C_1+C_c & -C_c \\ 0 & 0 & -C_c & C_2+C_c \end{pmatrix}, \mathscr{L} = (L), \quad \mathscr{G} = \begin{pmatrix} G_1 & 0 & -G_1 & 0 \\ 0 & G_3 & 0 & 0 \\ -G_1 & 0 & G_1+G_2 & -G_2 \\ 0 & 0 & -G_2 & G_2 \end{pmatrix}, \mathscr{E}_i = \begin{pmatrix} 0 \\ -1 \\ 0 \\ 1 \end{pmatrix} \tag{14}$$

$$\mathscr{E}_v = \begin{pmatrix} 1 & 0 \\ 0 & 1 \\ 0 & 0 \\ 0 & 0 \end{pmatrix}, \quad \mathscr{B} = \begin{pmatrix} -1 & 0 \\ 0 & -1 \end{pmatrix}, \mathscr{B}_v = -\mathscr{B} \tag{15}$$

Matrices (14), (15) are reduced either in first order form using SPRIM/IOPOR according to Sect. 3.2. Here we reduce the circuit with SPRIM/IOPOR and synthesize it by unstamping via RLCSYN. Note that there is an L directly connected to the second input node v_4, thus assumption 2. from RLCSYN is not satisfied. We thus reduce and synthesize the single-input-single-output version of (11) only, where the second input i_2 is removed. Therefore the new incidence matrices are:

$$\mathscr{E}_{v_1} = \begin{pmatrix} 1 \\ 0 \\ 0 \\ 0 \end{pmatrix},\ \mathscr{B}_1 = \begin{pmatrix} -1 \end{pmatrix},\ \mathscr{B}_{v_1} = -\mathscr{B}_1. \tag{16}$$

We choose an underlying PRIMA projection matrix $\mathbf{V} \in \mathbb{C}^{n\times k}$ spanning a $k = 2$-dimensional Krylov subspace (with expansion point $s_0 = 0$). According to Sect. 3.2, after splitting $\mathbf{V}$ and appropriate re-orthonormalization, the dimensions of the input-output structure preserving partitioning are :

$$n_1 = 1,\ n_2 = 3,\ n_l = 1,\ k_2 = 2,\ k_3 = 1, \tag{17}$$

and the SPRIM/IOPOR projection is:

$$\widetilde{\mathbf{W}} = \left(\begin{array}{ccc|c} 1 & 0 & 0 & 0 \\ 0 & 4.082\cdot 10^{-1} & -4.861\cdot 10^{-1} & 0 \\ 0 & 8.164\cdot 10^{-1} & 5.729\cdot 10^{-1} & 0 \\ 0 & 4.082\cdot 10^{-1} & -6.597\cdot 10^{-1} & 0 \\ \hline 0 & 0 & 0 & 1 \end{array}\right) \in \mathbb{C}^{5\times 4},\ \text{with } \mathbf{W} \in \mathbb{C}^{4\times 3}. \tag{18}$$

After diagonalization and regularization, the SPRIM/IOPOR reduced system matrices in (10) are:

$$\widetilde{\mathscr{C}} = \begin{pmatrix} 0 & 0 & 0 \\ 0 & 1.749\cdot 10^{-5} & -5.052\cdot 10^{-5} \\ 0 & -5.052\cdot 10^{-5} & 1.527\cdot 10^{-4} \end{pmatrix},\ \widetilde{\mathscr{G}} = \begin{pmatrix} 1 & 8.165\cdot 10^{-2} & -5.729\cdot 10^{-2} \\ 8.165\cdot 10^{-2} & 9.999\cdot 10^{-2} & -7.726\cdot 10^{-2} \\ -5.7295\cdot 10^{-2} & -7.7265\cdot 10^{-2} & 2.084\cdot 10^{-1} \end{pmatrix}$$
$$\widetilde{\Gamma} = \begin{pmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 30.14 \end{pmatrix},\ \widetilde{\mathscr{E}}_{v_1} = \begin{pmatrix} 1 \\ 0 \\ 0 \end{pmatrix} \tag{19}$$

Reduced matrices (19) are now unstamped individually using RLCSYN. The reduced system dimension in second order form is thus $N = 3$, indicating that the reduced netlist will have 3 nodes and an additional ground node. In the following, we denote by $M_{i,j}\ i = 1\ldots N,\ j = 0\ldots N-1$ a circuit element connected between nodes (i, j) in the resulting netlist. M represents a circuit element of the type: R,L,C or current source J.

By unstamping $\widetilde{\mathscr{G}}$, we obtain the following R values (for simplicity only 4 figures behind the period are shown here, nevertheless in implementation they are computed with machine precision $\varepsilon = 10^{-16}$):

$$R_{1,0} = \left[\sum_{k=1}^{3} \widetilde{\mathscr{G}}_{(1,k)}\right]^{-1} = 8.0417\ \Omega,\ R_{1,2} = -\left[\widetilde{\mathscr{G}}_{(1,2)}\right]^{-1} = -12.247\ \Omega,\ R_{1,3} = -\left[\widetilde{\mathscr{G}}_{(1,3)}\right]^{-1} = 17.452\ \Omega,$$
$$R_{2,0} = \left[\sum_{k=1}^{3} \widetilde{\mathscr{G}}_{(2,k)}\right]^{-1} = 9.5798\ \Omega,\ R_{2,3} = -\left[\widetilde{\mathscr{G}}_{(2,3)}\right]^{-1} = 12.942\ \Omega,\ R_{3,0} = \left[\sum_{k=1}^{3} \widetilde{\mathscr{G}}_{(3,k)}\right]^{-1} = 13.535\ \Omega.$$

By unstamping $\widetilde{\mathscr{C}}$, we obtain the following C values:

$$C_{2,0} = \sum_{k=1}^{3} \widetilde{\mathscr{C}}_{(2,k)} = -3.3026\cdot 10^{-5}\ F,\ C_{2,3} = -\widetilde{\mathscr{C}}_{(2,3)} = 5.0526\cdot 10^{-5},\ F,\ C_{3,0} = \left[\sum_{k=1}^{3} \widetilde{\mathscr{C}}_{(3,k)}\right]^{-1} = 1.0221\cdot 10^{-4}\ F.$$

By unstamping $\widetilde{\Gamma}$, we obtain the following L values:

$$L_{3,0} = \left[\sum_{k=1}^{3} \widetilde{\Gamma}_{(3,k)}\right]^{-1} = 3.317 \cdot 10^{-2}\ H.$$

By unstamping $\widetilde{\mathscr{E}}_{v_1}$, we obtain the current source $J_{1,0}$ of amplitude 1 A.

The Pstar [31] equivalent netlist is shown below:.

```
circuit;
     r r_1_0 (1, 0) 8.0417250765565598e+000;
     r r_1_2 (1, 2) -1.2247448713915894e+001;
     r r_1_3 (1, 3) 1.7452546181796258e+001;
     r r_2_0 (2, 0) 9.5798755840972589e+000;
     r r_2_3 (2, 3) 1.2942609947762115e+001;
     r r_3_0 (3, 0) 1.3535652691596653e+001;
     l l_3_0 (3, 0) 3.3170000000000033e-002;
     c c_2_0 (2, 0) -3.3026513336014821e-005;
     c c_2_3 (2, 3) 5.0526513336014765e-005;
     c c_3_0 (3, 0) 1.0221180442099465e-004;
     j j_1 (1, 0) sw(1, 0);
     c: Set node 1 as output: vn(1);
     c: Resistors 6;
     c: Capacitors 3;
     c: Inductors 1;
end;
```

Table 2 summarizes the reduction and synthesis results. Even though the number of internal variables (states) generated by the simulator is smaller for the SPRIM/IOPOR model than for the original, the number of circuit elements generated by RLCSYN is larger in the reduced model than in the original. Fig. 4 shows that approximation with SPRIM/IOPOR is more accurate than with PRIMA. The Pstar simulation of the RLCSYN synthesized model also matches the MATLAB simulation of the reduced transfer function.

Table 2 Input impedance reduction (SPRIM/IOPOR) and synthesis (RLCSYN)

System	Dimension	R	C	L	States	Inputs/Outputs
Original	5	3	3	1	5	1
SPRIM/IOPOR	4	6	3	1	4	1

4.2 SISO RLC network

We reduce the SISO *RLC* transmission line in Fig. 5. Note that the circuit is driven by the voltage **u**, thus it is of admittance type (4). The admittance simulation of the model reduced with the *dominant spectral zero method (Dominant SZM) [16, 30]*, synthesized with the Foster approach, is shown in Fig. 7. The behavior of the original model is well approximated for the entire frequency range, and can also reproduce oscillations at dominant frequency points.

The benefit of the admittance-to-impedance transformation described in Sect. 3.1 is seen in Fig. 8. By reducing the system in impedance form with SPRIM/IOPOR

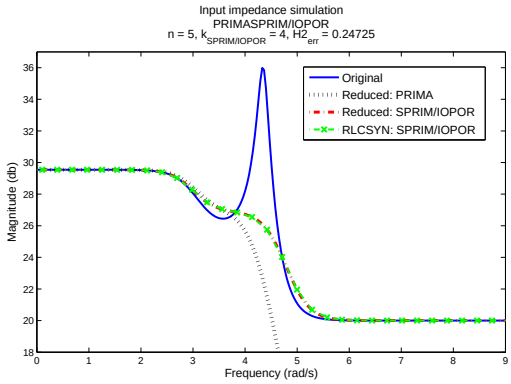

Fig. 4 Original, reduced and synthesized systems for the circuit in Fig. 3. The reduced (PRIMA, SPRIM/IOPOR) and synthesized systems match but miss the peak around 4.5 rad/s.

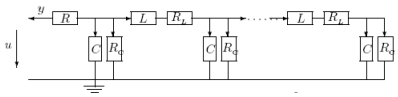

Fig. 5 Transmission line from Sect. 4.2

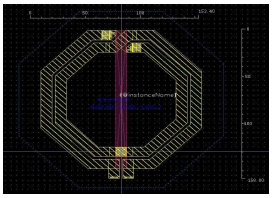

Fig. 6 Coil structre from Sect. 4.3

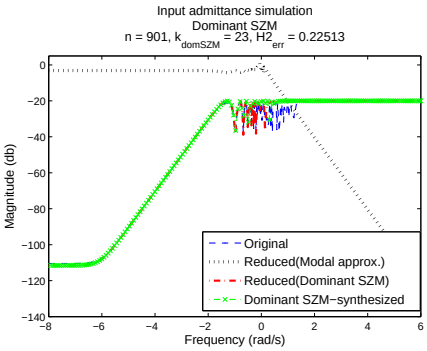

Fig. 7 Input admittance transfer function: original, reduced with Dominant SZM in admittance form and synthesized with Foster admittance

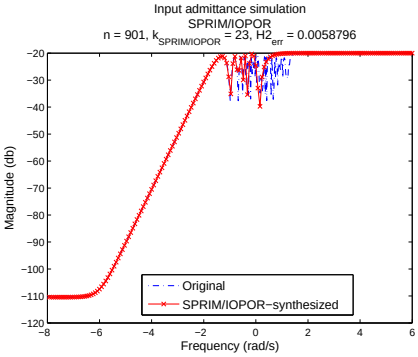

Fig. 8 Input admittance transfer function: original and synthesized SPRIM/IOPOR model (via impedance), after reconnecting the voltage source at the input terminal

and synthesizing (7) [using the second order form (10)] with RLCSYN [28], we are able to recover the reduced admittance (8) as well. The approximation is good for the entire frequency range.

4.3 *MIMO RLC* network

We reduce the MIMO *RLC* netlist resulting from the parasitic extraction [12] of the coil structure in Fig. 6. The model has 4 pins (external nodes). Pin 4 is connected to other circuit nodes only via *C*'s, which causes the original model (6) to have a pole at 0. The example shows that the SPRIM/IOPOR model preserves the terminals and is synthesizable with RLCSYN without controlled sources

Fig. 9 shows the simulation of the transfer function from input 4 to output 4. SPRIM/IOPOR is more accurate around DC than PRIMA. Another alternative is to ground pin 4 prior to reduction. As seen from Fig. 10, SPRIM/IOPOR applied on the remaining 3-terminal system gives better approximation than PRIMA for the entire frequency range. With pin 4 grounded however, we loose the ability to (re)connect the synthesized model in simulation via all the terminals.

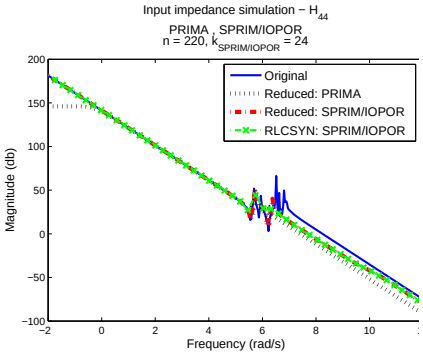

Fig. 9 Input impedance transfer function with "v_4" kept: $\mathbf{H}_{44}$ for PRIMA, SPRIM/IOPOR and RLCSYN realization

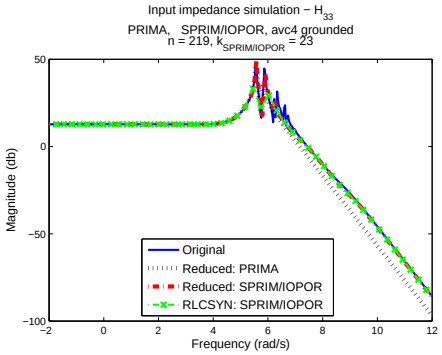

Fig. 10 Input impedance transfer function with "v_4" grounded: $\mathbf{H}_{33}$ for PRIMA, SPRIM/IOPOR and RLCSYN realization

5 Conclusions and outlook

A framework for realizing reduced mathematical models into *RLC* netlists was developed. Model reduction by projection for *RLC* circuits was described and associated with two synthesis approaches: Foster realization (for SISO transfer functions) and RLCSYN [28] synthesis by unstamping (for MIMO systems). An admittance-to-impedance conversion was prosed as a pre-model reduction step and shown to enable synthesis without controlled sources. The approaches were tested on several examples. Future research will investigate reduction and synthesis methods for *RCLK* circuits with many terminals, while developments on sparsity-preserving model reduction for multi-terminal *RC* circuits can be found in [29].

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