Model reduction for multi-terminal RC circuits

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Outline

1. Introduction
   - Motivation from electronics industry

2. MOR for multi-terminal circuits
   - Circuit modelling
   - General MOR framework
   - Multi-terminal MOR

3. Results
   - Netlist TL1
     - Circuit simulations
   - Netlist TL3

4. Summary

5. Bibliography
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Smaller feature sizes but increasing complexity

Parasitic interconnect
- dominates complexity of VLSI designs
- electromagnetic coupling effects
  - circuit performance
  - power
- inadequate for simulations
  - memory capacity, CPU time

Solution
Interconnect modelling and reduction
- synthesis, optimization, verification

Intel 4004. First microprocessor (1971)
MOR for electrical circuits

Original system

\[ \Sigma(C, G, B, B^T, D) \]

Large matrices \( n = 1M \)

Sparse

Reduced system

\[ \widehat{\Sigma}(\widehat{C}, \widehat{G}, \widehat{B}, \widehat{B}^T, D) \]

Small matrices \( \widehat{n} = 1k \)

Ideally Sparse

**Extraction**

Original circuit

- \# R = 1M
- \# C = 1M
- \# L = 1M
- \# nodes = 1M
- \# terminals = 10k

Full Simulation

- long CPU time
- numerical hurdles

Model Reduction

Modified nodal analysis

Reduced circuit

- \# R = 1k
- \# C = 1k
- \# L = 1k
- \# nodes = 1k
- \# terminals = 10k

Simulation

Network synthesis

Original system

- \# R = 1M
- \# C = 1M
- \# L = 1M
- \# nodes = 1M
- \# terminals = 10k

Full Simulation

- long CPU time
- numerical hurdles
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Modified nodal analysis (MNA) of *RLC* circuits

From Kirchoff’s current and voltage laws, and the branch constitutive equations

**Dynamical system (differential algebraic)**

\[
\begin{pmatrix}
C & 0 \\
0 & L
\end{pmatrix} \frac{d}{dt} \begin{pmatrix}
v(t) \\
i_L(t)
\end{pmatrix} + \begin{pmatrix}
G & E_i \\
-E_i^* & 0
\end{pmatrix} \begin{pmatrix}
v(t) \\
i_L(t)
\end{pmatrix} = \begin{pmatrix}
E_v \\
0
\end{pmatrix} i_{in}(t)
\]

- \(x\) internal variables: node voltages and currents through \(Ls\)
- \(i_{in}\) system inputs: currents injected into terminals
- \(y\) system outputs: voltage drops at terminals
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Model order reduction

Given original system $\Sigma$: dimension $n$, $p$ terminals

\[
\begin{align*}
E \dot{x}(t) &= A \ x(t) + B \ u(t) \\
y(t) &= C \ x(t) + D \ u(t)
\end{align*}
\]

$\Sigma = \begin{bmatrix} (A, E) & B \\ C & D \end{bmatrix}$

$x \in \mathbb{R}^{n \times 1}$, $E \in \mathbb{R}^{n \times n}$, $A \in \mathbb{R}^{n \times n}$, $B \in \mathbb{R}^{n \times m}$, $C \in \mathbb{R}^{p \times n}$, $D \in \mathbb{R}^{p \times m}$

Find reduced $\hat{\Sigma}$: dimension $k$, $p$ terminals, $p \leq k \ll n$

\[
\begin{align*}
\hat{E} \dot{\hat{x}}(t) &= \hat{A} \ \hat{x}(t) + \hat{B} \ u(t) \\
\hat{y}(t) &= \hat{C} \ \hat{x}(t) + D \ u(t)
\end{align*}
\]

$\hat{\Sigma} = \begin{bmatrix} (\hat{A}, \hat{E}) & \hat{B} \\ \hat{C} & D \end{bmatrix}$

$\hat{x} \in \mathbb{R}^{k \times 1}$, $\hat{E} \in \mathbb{R}^{k \times k}$, $\hat{A} \in \mathbb{R}^{k \times k}$, $\hat{B} \in \mathbb{R}^{k \times m}$, $\hat{C} \in \mathbb{R}^{p \times k}$

Construct $W, V$ to project $\Sigma$ on a $k$-dimensional subspace

$\hat{E} = W^{*}E V$, $\hat{A} = W^{*} A V$, $\hat{B} = W^{*} B$, $\hat{C} = CV$, $D = D$
Challenges in MOR

The usual targets

- achieving **accuracy** and **small dimensionality**
- preserving system properties: **stability**, **passivity**

New requirements for multi-terminal circuits

Critical for (re)simulation:

- preserving **structure** $\rightarrow$ convenient **synthesized models**
- preserving **sparsity** [few circuit elements] $\rightarrow$ memory and CPU requirements
How to meet MOR challenges

\[ \hat{E} = W^*EV, \quad \hat{A} = W^*AV, \quad \hat{B} = W^*B, \quad \hat{C} = CV, \quad D = D \]

\[ V, W \in \mathbb{C}^{n \times k}, \quad k \geq p, \quad p = \# \text{terminals} \]

Existing methods: Krylov/SVD-/EVD-based

- \( V, W \) satisfy the usual targets: accuracy, stability, passivity
- when \( p > 100 \), \( \hat{E}, \hat{A} \) are dense \( \rightarrow \) expensive to re-simulate!

New methods for multi-terminal circuits

- introduce graph-theoretical tools \( \rightarrow \) \( \hat{E}, \hat{A} \) with preserved structure & sparsity
- maintain the accuracy, stability, passivity requirements
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Sparse reduction of $R$ networks

[Rommes, Schilders: IEEE TCAD ’10]

[Rommes ’09 - COMSON MOR School]

Figure: Left: 59 nodes, 1711 resistors. Right: 64 nodes, 721 resistors

- Left: eliminate all internal nodes
- Right: preserve five internal nodes
- Selective (AMD) elimination reduces fill-in
- Terminals are preserved
Reducing large circuits with many terminals

**Candidates:** circuits with $O(10^3)$ nodes and $O(10^2)$ terminals (and beyond!)

**Divide**

Partition network graph into smaller sub-networks
- identifies **structure**
- fewer #nodes and #terminals per sub-network
- reduction is simplified algorithmically and computationally

**Conquer**

Reduce sub-networks individually
- can use an MOR method of choice
- allows better control on **sparsity**
Multi-terminal RC transmission line

← RC network as a graph
[shown are only R connections]

- $n = 3254$ nodes
- $p = 22$ terminals
- blue and green nodes are connected also to Cs
- 6 sub-networks are identified
**MOR for multi-terminal RC: “how to”**

**Divide**

1. **graph-based network partitioning** (strongly connected components, bi-connected components etc.)

**Conquer**

Per sub-network:

2. partition nodes & matrices
   - selected nodes: $x_S \in \mathbb{R}^{p+m}$ (terminals + some internal)
   - remaining nodes: $x_R \in \mathbb{R}^{n-m}$ internal nodes

3. reduce $x_R$, keep $x_S$

   *Advanced option: fill-in minimizing node reorderings $\rightarrow$ improved sparsity*

Based on method for $R$-networks [Rommes, Schilders: IEEE TCAD ’10]
RC netlist reduction: the maths

[I., Rommes: COMSON ’09]

On full circuit or per sub-network:

Original circuit model: $G, C \in \mathbb{R}^{n \times n}$, $B \in \mathbb{R}^{n \times p}$

From MNA circuit equations: $(G + sC)x = Bu$, partition $x$ in:

$$
\begin{pmatrix}
G_R & G_K \\
G_K^T & G_S
\end{pmatrix} + s
\begin{pmatrix}
C_R & C_K \\
C_K^T & C_S
\end{pmatrix}
\begin{pmatrix}
x_R \\
x_S
\end{pmatrix} =
\begin{pmatrix}
0 \\
B_S
\end{pmatrix} u.
$$

- Moment revealing transformation
  
  [Kerns, Yang: IEEE TCAD ’97]: $x =
\begin{bmatrix}
I & -G_R^{-1}G_K \\
0 & I
\end{bmatrix}$

- $G' = X^T GX$, $C' = X^T CX$, $B' = X^T B$, $x' = X^T x$
**RC netlist reduction: the maths ...**

**Transformed model:** \( \mathbf{G}', \mathbf{C}' \in \mathbb{R}^{n \times n}, \mathbf{B}' \in \mathbb{R}^{n \times p} \)

\[
\mathbf{G}' = \begin{bmatrix} \mathbf{G}_R & 0 \\ 0 & \mathbf{G}'_S \end{bmatrix}, \quad \mathbf{C}' = \begin{bmatrix} \mathbf{C}_R & \mathbf{C}'_K \\ \mathbf{C}'_K & \mathbf{C}'_S \end{bmatrix}, \quad \mathbf{B}' = \begin{bmatrix} 0 \\ \mathbf{B}_S \end{bmatrix}, \quad \mathbf{x}' = \begin{bmatrix} \mathbf{x}_R \\ \mathbf{x}'_S \end{bmatrix}
\]

\[
\begin{align*}
\mathbf{G}'_S &= \mathbf{G}_S - \mathbf{G}_K^T \mathbf{G}_K^{-1} \mathbf{G}_K, \\
\mathbf{C}'_S &= \mathbf{C}_S + \mathbf{V}^T \mathbf{C}_R \mathbf{V} + \mathbf{V}^T \mathbf{C}_K + \mathbf{C}_K^T \mathbf{V}, \\
\mathbf{C}'_K &= \mathbf{C}_K + \mathbf{C}_R \mathbf{V}
\end{align*}
\]

\[
\begin{bmatrix} \mathbf{G}'_S + s \mathbf{C}'_S \end{bmatrix} - \begin{bmatrix} s^2 \mathbf{C}'_K \mathbf{G}_R + s \mathbf{C}_R \end{bmatrix}^{-1} \mathbf{C}'_K \mathbf{x}'_S = \mathbf{B}_S \mathbf{u}
\]

Multiport admittance: \( \mathbf{Y}'_S(s) \) already captures first 2 moments!

**Reduced circuit model:** \( \hat{\mathbf{G}}, \hat{\mathbf{C}} \in \mathbb{R}^{k \times k} \quad p \leq k \ll n \)

\[
\hat{\mathbf{G}} = \mathbf{G}'_S, \quad \hat{\mathbf{C}} = \mathbf{C}'_S, \quad \hat{\mathbf{B}} = \mathbf{B}_S, \quad \hat{\mathbf{x}} = \mathbf{x}'_S \\
(\hat{\mathbf{G}} + s \hat{\mathbf{C}}) \hat{\mathbf{x}} = \hat{\mathbf{B}} \mathbf{u}
\]
**RC netlist reduction: strategy & maths**

**Benefits**
- moment preservation → necessary for accuracy
- guaranteed stability and passivity → necessary in simulation

**Limitations**
1. recall transform involving $V = G_R^{-1} G_K$ → costly for $O(10^4)$ nodes and beyond
2. fill-in in $G_S'$ and $C_S'$ → too many circuit elements!

**Solution**
- structured reduction (i.e. per sub-networks) to resolve [1.]
- fill-in minimizing node reorderings to resolve [2.]
Industrial testcases

Parasitic extraction \( RC \) models of a Low Noise Amplifier circuit (C45 technology)\(^1\)

<table>
<thead>
<tr>
<th>Inventory</th>
<th>TL 1</th>
<th></th>
<th>TL 2</th>
<th></th>
<th>TL 3</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Original</td>
<td>Red</td>
<td>Original</td>
<td>Red</td>
<td>Original</td>
<td>Red</td>
</tr>
<tr>
<td>#ext. nodes</td>
<td>79</td>
<td></td>
<td>75</td>
<td></td>
<td>79</td>
<td></td>
</tr>
<tr>
<td>#int. nodes</td>
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<td>0</td>
<td>33818</td>
<td>0</td>
<td>27962</td>
<td>0</td>
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<tr>
<td>#resistors</td>
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<td>117</td>
<td>81843</td>
<td>99</td>
<td>66068</td>
<td>117</td>
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<tr>
<td>#capacitors</td>
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<td>1047</td>
<td>12145</td>
<td>920</td>
<td>9786</td>
<td>1032</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Analysis</th>
<th>CPU time</th>
</tr>
</thead>
<tbody>
<tr>
<td>AC</td>
<td>65.83 s</td>
</tr>
<tr>
<td>Noise</td>
<td>59.68 s</td>
</tr>
<tr>
<td>SP</td>
<td>82.81 s</td>
</tr>
<tr>
<td>PSS</td>
<td>793.13 s</td>
</tr>
</tbody>
</table>

| Speed up   | > 270x   | > 127x  | ∞        |

\(^1\)Thanks: Gerben de Jong, Dennis Jeurissen (SDR Project, NXP Semiconductors)

\(^2\)No DC solution found (no convergence)
TL1 original matrices: $n = 29885$, $p = 79$
TL1 reduced matrices: $k = 79, \ p = 79$

Maximum reduction $\leftrightarrow$ eliminate all nodes except terminals

$\hat{G}$

$\hat{C}$
TL1 reduced matrices: $k = 2867, \ p = 79$

Partial reduction $\leftrightarrow$ preserve some internal nodes

$\hat{G}$

$\hat{C}$
## TL1: Reduction Summary

2 reduced netlists: **maximum reduced** and **partially reduced**

<table>
<thead>
<tr>
<th>Inventory</th>
<th>Original</th>
<th>Reduced (max.)</th>
<th>Perc.</th>
<th>Reduced (partial)</th>
<th>Perc.</th>
</tr>
</thead>
<tbody>
<tr>
<td>#ext. nodes</td>
<td>79</td>
<td>79</td>
<td>100%</td>
<td>79</td>
<td>90.2%</td>
</tr>
<tr>
<td>#int. nodes</td>
<td>29806</td>
<td>0</td>
<td>100%</td>
<td>2903</td>
<td>93.9%</td>
</tr>
<tr>
<td>#resistors</td>
<td>70338</td>
<td>117</td>
<td>99.8%</td>
<td>4248</td>
<td>93.9%</td>
</tr>
<tr>
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<td>1047</td>
<td>91.3%</td>
<td>4382</td>
<td>63.6%</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Analysis</th>
<th>CPU time</th>
<th>Speed Up</th>
<th>CPU time</th>
<th>Speed Up</th>
</tr>
</thead>
<tbody>
<tr>
<td>AC</td>
<td>65.83 s</td>
<td>0.12 s</td>
<td>~548x</td>
<td>1.46 s</td>
</tr>
<tr>
<td>Noise</td>
<td>59.68 s</td>
<td>0.13 s</td>
<td>~450x</td>
<td>1.71 s</td>
</tr>
<tr>
<td>SP</td>
<td>82.81 s</td>
<td>0.21 s</td>
<td>~394x</td>
<td>2.74 s</td>
</tr>
<tr>
<td>PSS</td>
<td>793.13 s</td>
<td>2.93 s</td>
<td>~270x</td>
<td>17.46 s</td>
</tr>
</tbody>
</table>
AC analysis - node “in”: magnitude

Comparison: original, maximum and partially reduced
PSS analysis, time domain - node “out”

Comparison: original, maximum and partially reduced
PSS analysis, freq. domain - node “out”

Comparison: original, maximum and partially reduced
[matched fundamental harmonics at 2 GHz]
Noise analysis - NF

Comparison: original, maximum and partially reduced → perfect match for range of interest [up to 10GHz]
Reduction Summary: TL3

Immediate benefit from reduction!

- Original simulation not possible → error “NO DC solution found, no convergence”
- Simulation possible after reduction [quality “predicted” from experiments with TL1 and TL2]

<table>
<thead>
<tr>
<th>Inventory</th>
<th>Original</th>
<th>Reduced</th>
<th>Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>#ext. nodes</td>
<td>79</td>
<td></td>
<td></td>
</tr>
<tr>
<td>#int. nodes</td>
<td>27962</td>
<td>0</td>
<td>100%</td>
</tr>
<tr>
<td>#resistors</td>
<td>66068</td>
<td>117</td>
<td>99.8%</td>
</tr>
<tr>
<td>#capacitors</td>
<td>9786</td>
<td>1032</td>
<td>89.5%</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Analysis</th>
<th>CPU time</th>
<th>Speed Up</th>
</tr>
</thead>
<tbody>
<tr>
<td>AC</td>
<td>NA(^3)</td>
<td>0.12 s</td>
</tr>
<tr>
<td>Noise</td>
<td>NA</td>
<td>0.14 s</td>
</tr>
<tr>
<td>SP</td>
<td>NA</td>
<td>0.22 s</td>
</tr>
<tr>
<td>PSS</td>
<td>NA</td>
<td>3.05 s</td>
</tr>
</tbody>
</table>

\(^3\)No DC solution found (no convergence)
TL3 reduced circuit simulations

**PSS: node “Vse2lse_0:2”**

Periodic Steady-State Analysis `pss`: time = (0 s → 5.26316 ns)

![Graph showing periodic steady-state analysis](image)

**Noise: NF**

Noise Analysis `noise`: freq = (10 MHz → 100 GHz)

![Graph showing noise analysis](image)
Summary

MOR for multi-terminal circuits

- electronics industry needs new MOR methods → structure identification and sparsity preservation
- divide and conquer strategy → efficiency from reducing smaller subnetworks individually
- **reduced netlists** for multi-terminal RC networks (up to 100 terminals)
  - significant reduction in \#nodes, \#Rs, \#Cs → much faster simulations
  - partial reduction possible → better approximation
- netlists beyond 100 terminals → in progress
For further reading


Rommes, J.: “Eigenvalue problems and model order reduction in the electronics industry,”
COMSON Autumn School on MOR, presented in Terschelling, the Netherlands, Sept. 21-25, 2009.


Ionutiu, R., Rommes, J.: “On synthesis of reduced order models”

Ionutiu, R., Rommes, J.: “Model order reduction for multi-terminal circuits,”