Communication protocols for modular FPGA-designs.

Background:

In course 2IN35 on VLSI-programming an asynchronous protocol to connect modules of multi-rate systems has been presented [1]. In the literature [2, 3] similar protocols have been defined in the context of SoC-design. All these protocols share the property that they can turn a standard synchronous design that adheres to very mild restrictions into a design obeying the protocol by the following operations. First, all modules are embedded in wrappers that present the protocol interface to the environment. Second, the modules thus wrapped are hooked up using special connectors.

Goals and task:

1. Develop Verilog wrappers and connectors for all protocols.
2. Compare the performance of systems, e.g. taken from 2IN35, under the various protocols.
3. Develop a Verilog preprocessor that automates the procedure sketched above.

References:


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Pre-requisites: Successful completion of the course 2IN35.

Assignment type: Master of Science thesis project (internal)

Planning: Starting date: asap

Status: Available