EINDHOVEN UNIVERSITY OF TECHNOLOGY

Department of Mathematics and Computer Science

Written examination Real-time software engineering (2IN70) - Part II: Real-time Architectures on Friday, April 15^{th} 2016, 18:00h-21:00h.

Hand-in the answers to this 2^{nd} part of the examination on separate sheets of paper, and make sure to put your name and identification number on the paper.

Read all the questions first. There are 4 questions in total. Points for each question are indicated between parentheses and sum up to 6 points. Many questions have a word limit, which must be observed. Good luck!

1. *Automotive domains and requirements*
   Five main functional domains have been distinguished for automotive, i.e. (*i*) powertrain, (*ii*) chassis, (*iii*) body (comfort), (*iv*) telematics/wireless, and (*v*) passive safety.

   (a) (0.5) Describe (in at most two sentences) how the *requirement* of *safety* differs qualitatively (e.g. low, high) for these domains.
   Answer: Slide 7 of `introduction` provides an overview. The safety requirements for (*i*) and (*ii*) are high, of (*iii*) and (*iv*) are low, and of (*v*) are very high.

   (b) (0.5) Describe (in at most three sentences) how the *requirement* of *timeliness/predictability* differs qualitatively for which these domains.
   Answer: See slide 27 and beyond of `introduction`. Because of the safety requirements, (*i*), (*ii*), and (*v*) have hard timing requirements and (*iii*) firm/soft timing requirements. Although (*iv*) has a low safety requirement, it also has hard timing requirements, because otherwise the connection may be lost.

2. *Microcontroller*

   (a) (1.0) Describe how a CPU executes instructions. *Hint*: describe the steps of a so-called *load-store ISA*.
   Answers: See slide 16 of `microcontroller`.

   (b) (0.5) Describe how programs can communicate with external devices via input and output ports in at most 3 sentences.
   Answer: See slide 22 of `microcontroller`. Keywords: ports are memory mapped, setup and control via control registers (also special memory addresses).

3. *Synchronization*

   (a) *Implementing mutual exclusion*:

      i. (0.5) Give a disadvantage of implementing mutual exclusion by disabling interrupts.
      Answer: see slide 5 of `synchronization`.

ii. (0.5) Give a disadvantage of implementing mutual exclusion by disabling the scheduler.
Answer: see slide 6 of `synchronization`.

(b) *Deadlock*:

i. (0.5) Describe the characteristics of a deadlock and give an example.
Answer: See slide 15 of `synchronization` and book.

ii. (0.5) Describe two approaches to avoid deadlocks.
Answer: See slide 17 + 19 of `synchronization` and book.

4. *Analysis*: The following table provides the characteristics of a task set $\mathcal{T}$.

	$T = D$	C
τ_1	4	2
τ_2	7	3
τ_3	23	1

(a) (0.5) A *sufficient* condition for schedulability of the three tasks that is given by

$$U^{\mathcal{T}} \leq n\left(2^{1/n} - 1\right), \tag{1}$$

where $n = |\mathcal{T}| = 3$. What can be concluded from the fact that this condition does not hold for $\mathcal{T}$, i.e. $U^{\mathcal{T}} \approx 0.97 > 3 \cdot \left(2^{1/3} - 1\right) \approx 0.78$?
Answer: $\mathcal{T}$ may but need not be schedulable.

(b) Assume fixed-priority pre-emptive scheduling, where τ_1 has highest and τ_3 has lowest priority.

i. (0.5) Draw a time line with a critical instant for task τ_3.
Answer: See Figure 1. Note that $WR_3 = 20 < D_3 = 23$.

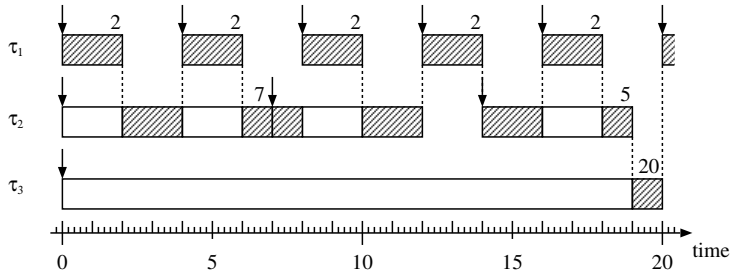

Figure 1: Time line with a critical instant for task τ_3.

ii. (0.5) Are all tasks of $\mathcal{T}$ schedulable?
Answer: From the timeline, we see $WR_1 = 2 < D_1 = 4$, $WR_2 = 7 \leq D_1 = 7$, and $WR_3 = 20 < D_3 = 23$. Hence, the taskset is schedulable.