Architecture of Distributed Systems

Homework Assignment 1

R. H. Mak

TU/e
Technische Universiteit Eindhoven
University of Technology

Where innovation starts
Exercise

Consider the models on the following slides and answer the following questions. Each model is provided with a hyperlink to acknowledge its source and for additional information.

1. What building blocks do you see? What do they represent? Are they conceptual (C) or physical (P)?
2. Same questions as 1, but now for connectors? Do not forget (C) or (P)!
3. To which views (1..*) does the model belong?
   Motivate why, and identify corresponding stakeholders and their concerns.
4. Which of the following EFRs are addressed (Y + motivation | N)?
   Performance/scalability, availability/reliability, security, maintainability, other?
5. Is there a concept of distribution (Y + motivation | N)?
6. Comment on the clarity/semantics of the diagram
   ☺ | ☹ | ☹ , plus motivation

Keep your answers crisp!
Taken from:
VICSDA: using virtual communities to secure service discovery and access
Taken from:
http://ithare.com/m mog-rtt-input-lag-and-how-to-mitigate-them/

Diagram:

- Presses Button (Clicks Mouse, ...)
- Sends "Button Pressed" message to Server
- Transit
- Processes Button Press, Updates Game World, sends "World Updated" message to all clients
- Transit
- Processes "World Updated" message and renders it
- Can See Result of Her Click

Player | Client | Internet | Server
--- | --- | --- | ---

Time:
- T1 = T0 + 5 ms
- T2 = T1 + 50 ms = T0 + 55 ms
- T3 = T2 + 50 ms = T0 + 105 ms
- T4 = T3 + (67 + 40) ms = T0 + 227 ms

* 67 ms for rendering lag, and 40 ms for display lag
** All times are for example purposes only, YMMV greatly

NOT REALLY PRACTICAL FOR FAST-PACED GAMES: SEE FIG VIII.2 FOR NECESSARY IMPROVEMENTS

Fig VII.1
Typical sources of interferences, causing errors detected by E2E protection:

**SW-related sources:**
- S1. Error in mostly generated RTE.
- S2. Error in partially generated and partially hand-coded COM.
- S3. Error in network stack.
- S4. Error in generated IOC or OS.

**HW-related sources:**
- H1. Microcontroller error during core/partition switch.
- H2. Failure of HW network.
- H3. Microcontroller failure during context switch (partition) or on the communication between cores.
Taken from:
https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=6298895
Taken from:
https://www.programiz.com/python-programming/package